X-611-64-183

TM X-55077

WIDE DYNAMIC RANGE PULSE HEIGHT ANALYZER WITH DATA COMPRESSION, COINCIDENCE LOGIC, AND DIGITAL READOUT CIRCUITS

JUNE 15, 1964

NASA
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

WIDE DYNAMIC RANGE PULSE HEIGHT ANALYZER WITH DATA COMPRESSION, COINCIDENCE LOGIC, AND DIGITAL READOUT CIRCUITS

S. Paull
C. Cancro
R. McGowan

Flight Data Systems Branch
Spacecraft Technology Division

June 15, 1964

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

WIDE DYNAMIC RANGE PULSE HEIGHT ANALYZER WITH DATA COMPRESSION, COINCIDENCE LOGIC, AND DIGITAL READOUT CIRCUITS

INTRODUCTION

33559

The Mark 6 Coincident Pulse A. to D. Converter and Readout System (ADCR-6) is a three-parameter pulse height analyzer employing amplitude range selection to give 6400 levels with coincidence logic and tape recorder readout circuits. The system is designed for Nuclear Abundance E vs dE/dx measurements on high altitude balloon flights. Three photomultiplier tubes in a scintillation telescope furnish signal pulses to the pulse height analyzer inputs identified as Channel A, Channel B, and Channel C. Pulse height analyzer operation is controlled by the coincidence logic circuits so that input pulse amplitude information on all three channels is fed to a 16-track tape recorder in digital form whenever simultaneous inputs occur on Channels A and B. The pulse amplitude information is contained in three 7-bit words plus index and multiplying factor bits. These are fed to the tape recorder as two 16-bit readouts for each recorded event. Each 7-bit word plus 2 bits to indicate a multiplying factor gives an accuracy of ∓4% or better over the dynamic range of 6400 to 1.

SYSTEM OPERATION

Figure 1 is a block diagram of the entire system showing the circuits divided into the following functional groups:

(1) Pulse Height Analyzer, Channel A

(2) Pulse Height Analyzer, Channel B

(3) Pulse Height Analyzer, Channel C

(4) Coincidence Logic Circuits

(5) Common Circuits, Busy Bistable and 500 kc Clock

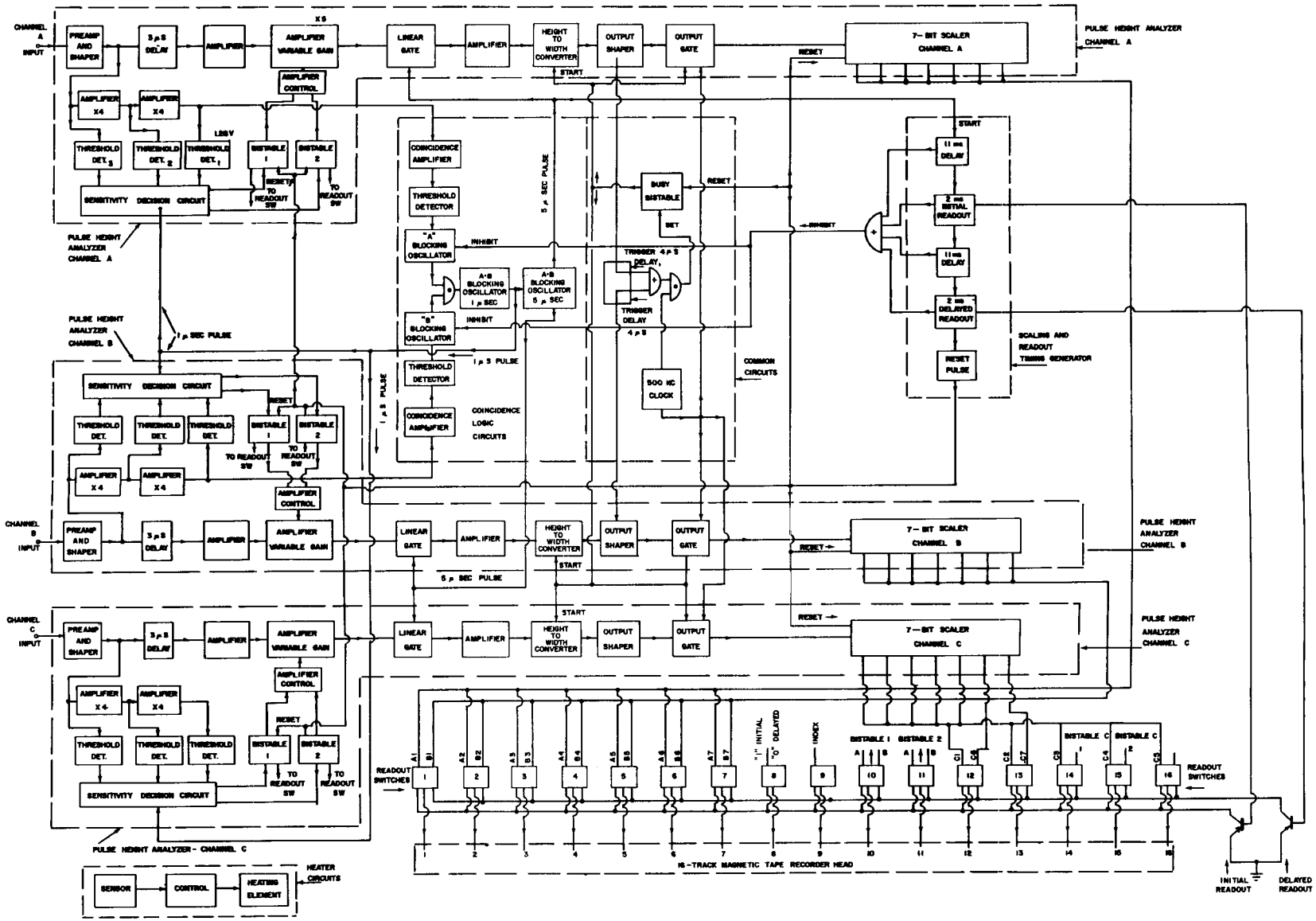


Figure 1–Three Parameter Coincident Pulse A. to D. Converter and Readout System Mark 6

(6) Scaling and Readout Timing Generator

(7) Readout Switches

(8) Heater Circuits

Pulse Height Analyzers. The three pulse height analyzer Channels (A, B, and C) are identical. An input signal to any one channel is a positive-going pulse with 1 to 2 microseconds rise time and approximately 7 microseconds exponential fall time to 1/2 peak amplitude. A digital output count proportional to input peak pulse amplitude is fed to the 7-bit scaler in each channel when and only when inputs on Channel A and Channel B are coincident. Minimum input pulse amplitude is 1 mv corresponding to an output count of 1. Maximum input pulse amplitude for linear operation is 6.4 volts, corresponding to an output count of 6400.

The preamplifier and Shaper section in the front end of each pulse height analyzer channel has an over-all gain of 0.8. The shaper is a delayed feedback circuit that reduces the input pulse width to 2 microseconds. Outputs from this section are fed to sensitivity setting amplifiers and threshold detectors, and also through a 3-microsecond delay to a variable-gain amplifier. The delay is included to allow time for the coincidence logic to function before the signal arrives at the linear gate. The gain of the variable-gain amplifier is set to one of four values (1, 4, 16, or 64) depending on the amplitude of the input signal. An appropriate multiplier is applied to the digital output count, as indicated by the condition of the two bistables which set the amplifier gain. This variable gain operation for input signals from 1 mv to 6.4 volts is illustrated in Table 1.

Table 1

Input Signal Amplitude Range	Amplifier Gain Setting	Linear Gate Input Signal	Digital Output Count	Multiplier
1 mv to 100 mv	64	40 mv to 4 v	1 to 100	1
100 mv to 400 mv	16	1 v to 4 v	25 to 100	4
400 mv to 1.6 v	4	1 v to 4 v	25 to 100	16
1.6 v to 6.4 v	1	1 v to 4 v	25 to 100	64

Signals that pass through the linear gate are applied to a sweep generator and output shaper. These circuits generate an output gate pulse whose duration is proportional to the applied signal amplitude. Each output gate pulse sends a burst of 500 kc clock pulses to the 7-bit scaler. The number of clock pulses in the burst is proportional to the input signal pulse amplitude.

Coincidence Logic. Signals from the Channel A preamplifier output are fed to the Channel A Coincidence amplifier and threshold detector. The threshold detector is adjusted to trigger the "A" blocking oscillator whenever the Channel A input from the scintillation telescope is at least 1 mv. Similarly, the Channel B coincidence amplifier and threshold detector are adjusted to trigger the "B" blocking oscillator whenever the Channel B input from the scintillation telescope is at least 1 mv.

Coincidence of a pulse from the "A" blocking oscillator and one from the "B" blocking oscillator triggers the 1 microsecond "A·B" blocking oscillator. This 1 microsecond pulse is fed to the sensitivity decision circuits in Channels A, B, and C to set the gain of the variable-gain amplifiers. It also triggers the second "A·B" blocking oscillator which furnishes a 5 microsecond pulse to unblock the linear gates in the three pulse height analyzer channels. The leading edge of this pulse triggers the Scaling and Readout Timing Generator.

Figure 2 illustrates the timing of the scaling action in the pulse height analyzers by showing the time relationship of signal pulses in the linear circuits, coincidence logic pulses, and output gating pulses. The timing is shown for the case where input signals on all three channels are equal. Timing of coincidence pulses for any other case of unequal signal pulses will depend on their relative amplitudes and on the threshold detector settings.

Scaling and Readout Timing. Timing of an A. to D. scaling and readout action is done with two identical magnetic core monostable multivibrators. Coincidence of pulses in channels A and B initiates timing action in the first multivibrator which puts out one complete cycle of an unbalanced square wave. The first portion of this square wave is a "scaling time" of 11 milliseconds during which input signals in the three pulse height analyzer channels are processed by the A. to D. circuits, and the digital information is fed to the three 7-bit scalers. The second portion of 2 milliseconds activates parallel readout of 12

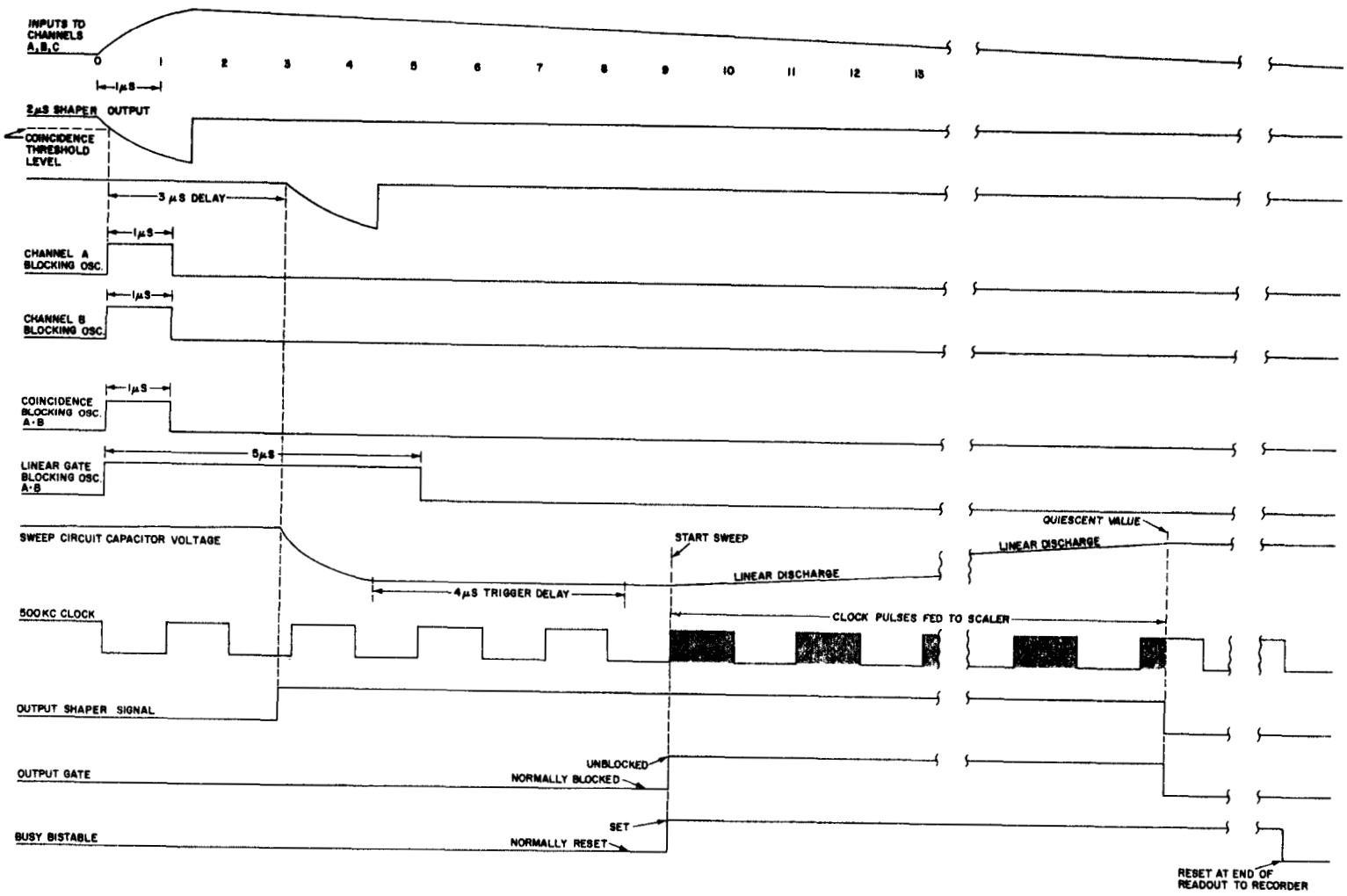


Figure 2–Scaling Action Timing

of these stored bits plus two index bits and two sensitivity bits into the 16 magnetic tape recorder heads. At the end of this initial readout, action is initiated in the second timing multivibrator which generates another unbalanced square wave cycle. The first portion of 11 milliseconds is a delay time to insure that spacing between words on the magnetic tape is adequate for clear data pick-off. The second portion of 2 milliseconds activates parallel readout of the remaining stored bits in the scalers plus sensitivity bits and index bits into the 16 magnetic tape recorder heads. Thus a complete event comprising pulse amplitude scaling on three pulse-height-analyzer channels is recorded as two 16-bit words on the magnetic tape in a 26 millisecond timing action as illustrated in the timing diagram, Figure 3.

During this 26 millisecond interval, the coincidence circuits are inhibited and the entire system is therefore insensitive to additional inputs. This limits the maximum possible event-rate capability of the system to input signals spaced no less than 26 milliseconds apart, that is, the maximum possible operating speed is 38.4 events per second.

CIRCUIT DESIGN

Pulse Height Analyzer Circuits

A number of amplifiers used repeatedly in the system are shown in block diagram form on the pulse height analyzer schematics to simplify discussion of circuit design. These amplifiers are the following:

(1) Amplifier Type 1b, Figure 4. This is a non-inverting amplifier operating with positive-going input and output signals. Overall gain is approximately

$$\frac{R_1+R_2}{R_2}$$

and can be set to values less than 6 by shunting R_1 with an appropriate resistance value.

(2) Amplifier Type 2 (c) and 2 (d), Figure 5. This circuit is similar to the type 1b except that p-n-p and n-p-n transistors are interchanged and D-C supply voltages are reversed. Lower circuit impedances have the effect of reducing phase shift from input to output. These circuits

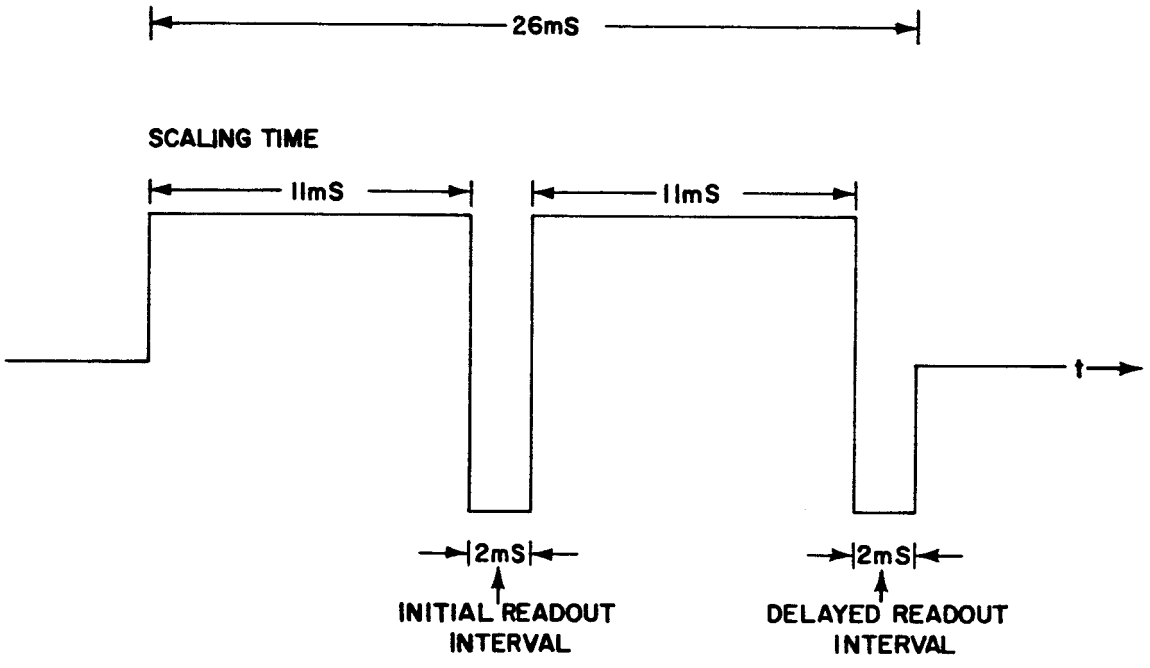


Figure 3–Timing Generator Operation

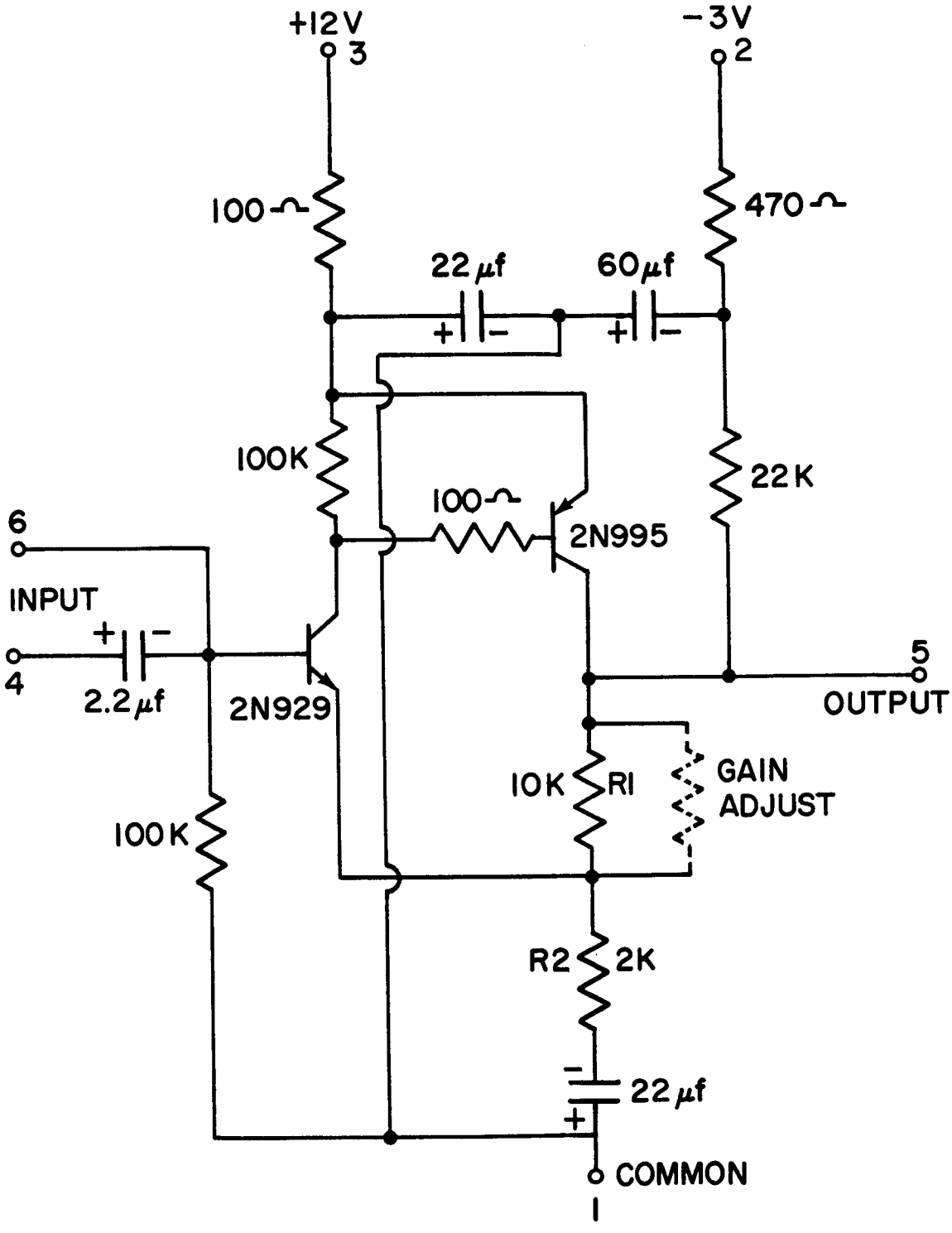


Figure 4—Amplifier Type 1b

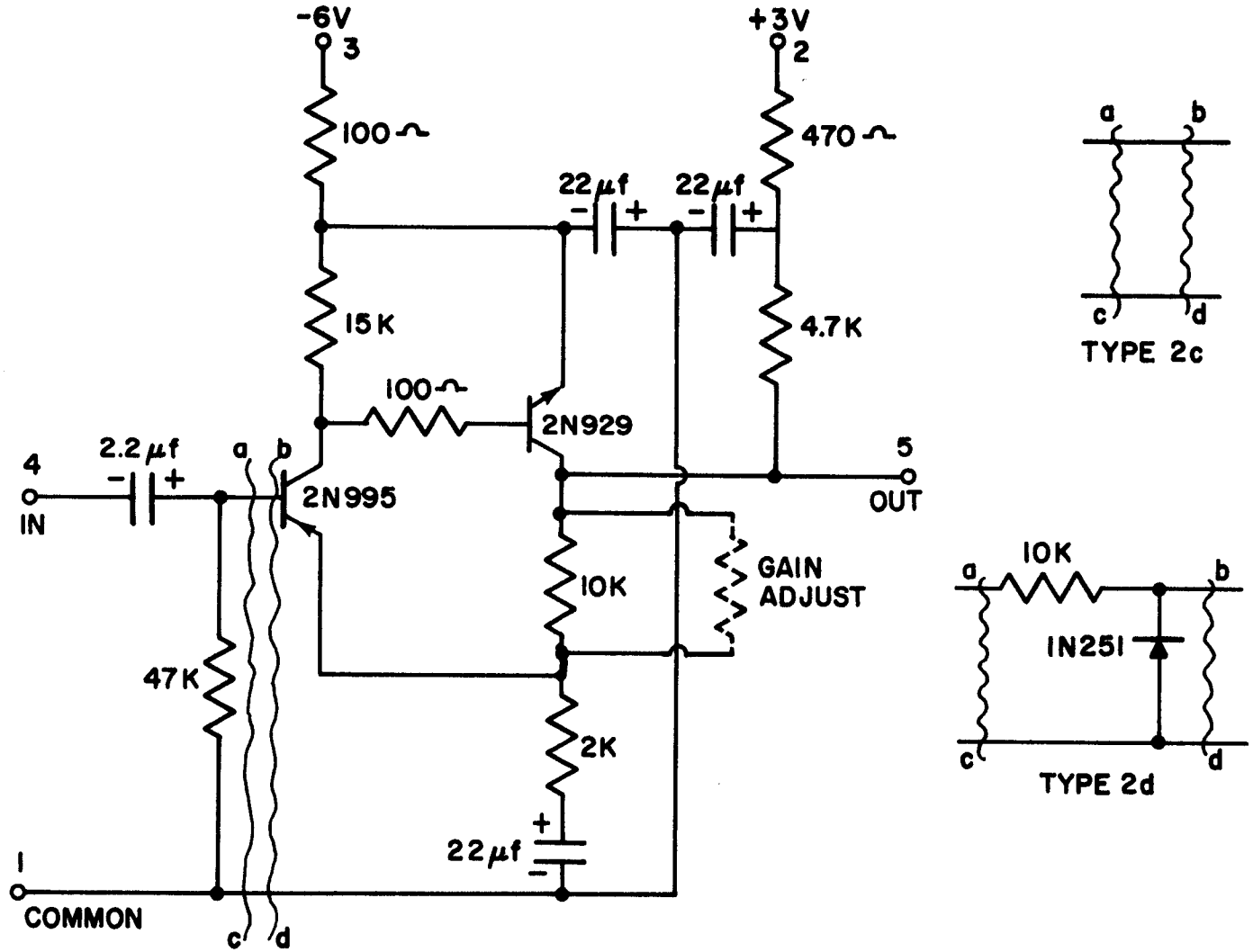


Figure 5–Amplifier, Type 2(c) and 2(d)

operate with negative-going input pulses and furnish negative-going output pulses. The type 2 (d) circuit includes diode limiting at the input to the first transistor to prevent saturation when input signals are large.

(3) Preamplifier and Shaper Section. The preamplifier and shaper section at the input end of each pulse height analyzer channel includes an amplifier, type 1b, a shaper, 2 microsecond, and an amplifier type 2c interconnected as shown in Figure 6. The shaper, 2 microsecond, Figure 7, is a two-stage amplifier with delayed negative feedback. Positive-going input pulses with approximately 2 microsecond rise time and greater than 7 microseconds fall time are shaped to give a very fast fall time. The beginning of the shaped fall time is determined by the delay line (2 microseconds), thus allowing pulses with rise time up to 2 microseconds to reach peak value before decaying. The shape of the output pulse decay is determined by adjusting shunting resistors across R_1 and R_2. The shaper circuit furnishes negative-going output pulses.

(4) Coincidence Logic Circuits. Interconnection of circuits performing the coincidence logic function is shown in Figure 8. The amplifiers type 2d have already been discussed in connection with the schematic of Figure 5. The other circuits in Figure 8 are shown in the following schematics:

Threshold Detector, Figure 9
Emitter Follower, Figure 10
Blocking Oscillator, Figure 11

The threshold detector, Figure 9, furnishes a positive 6 volt output pulse whenever a negative-going input pulse exceeds a threshold value determined by the "threshold level adjust" resistor setting. The threshold detector output drives the emitter follower shown in Figure 10.

The blocking oscillator, Figure 11, furnishes an output pulse determined by the pulse transformer design and the supply voltage. Pulse transformers are wound on Alladin Bobbin and Sleeve ferrite coil forms:

Bobbin No. 110-1097
Sleeve No. 110-1098

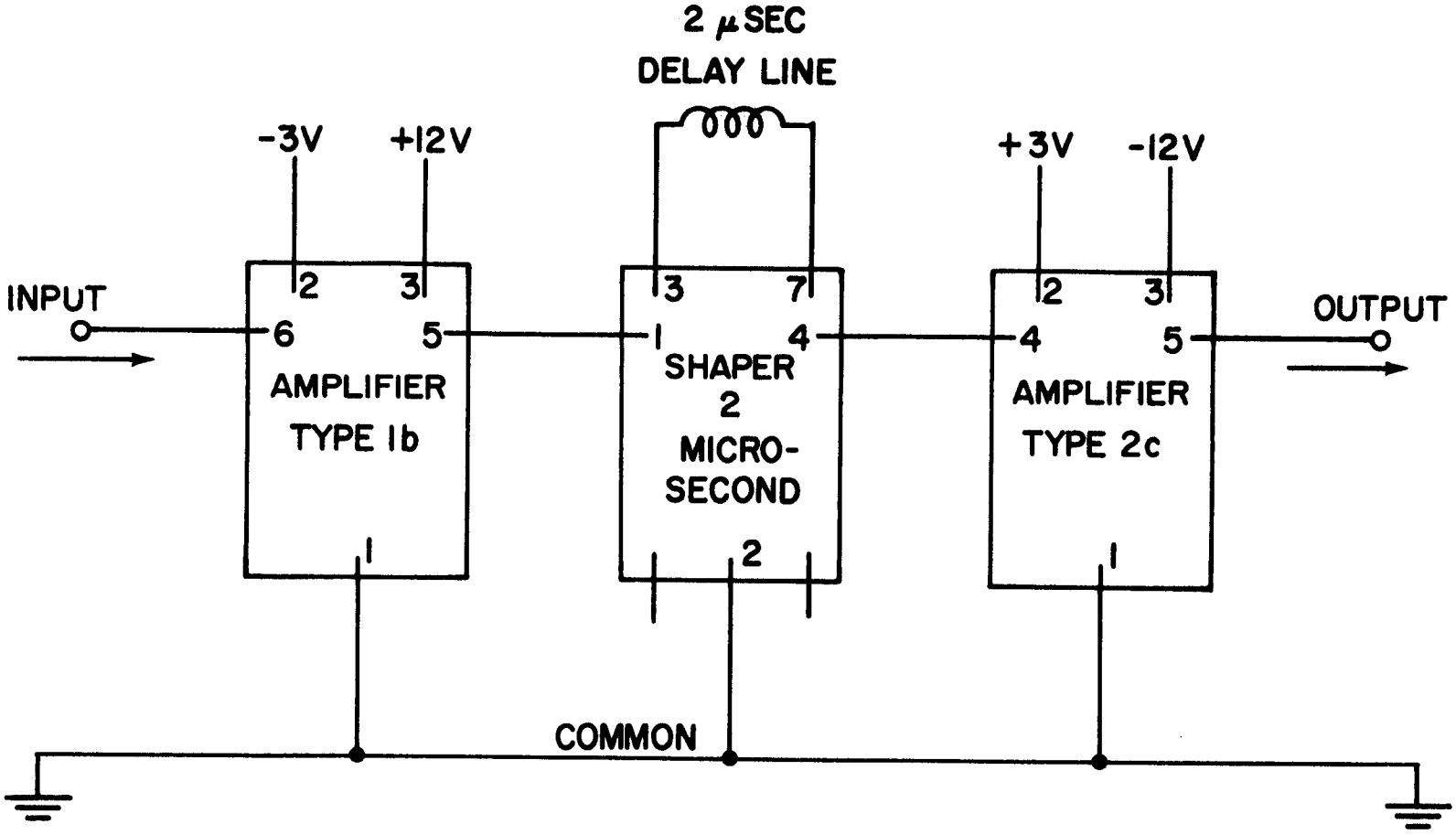


Figure 6–Preamplifier and Shaper Section

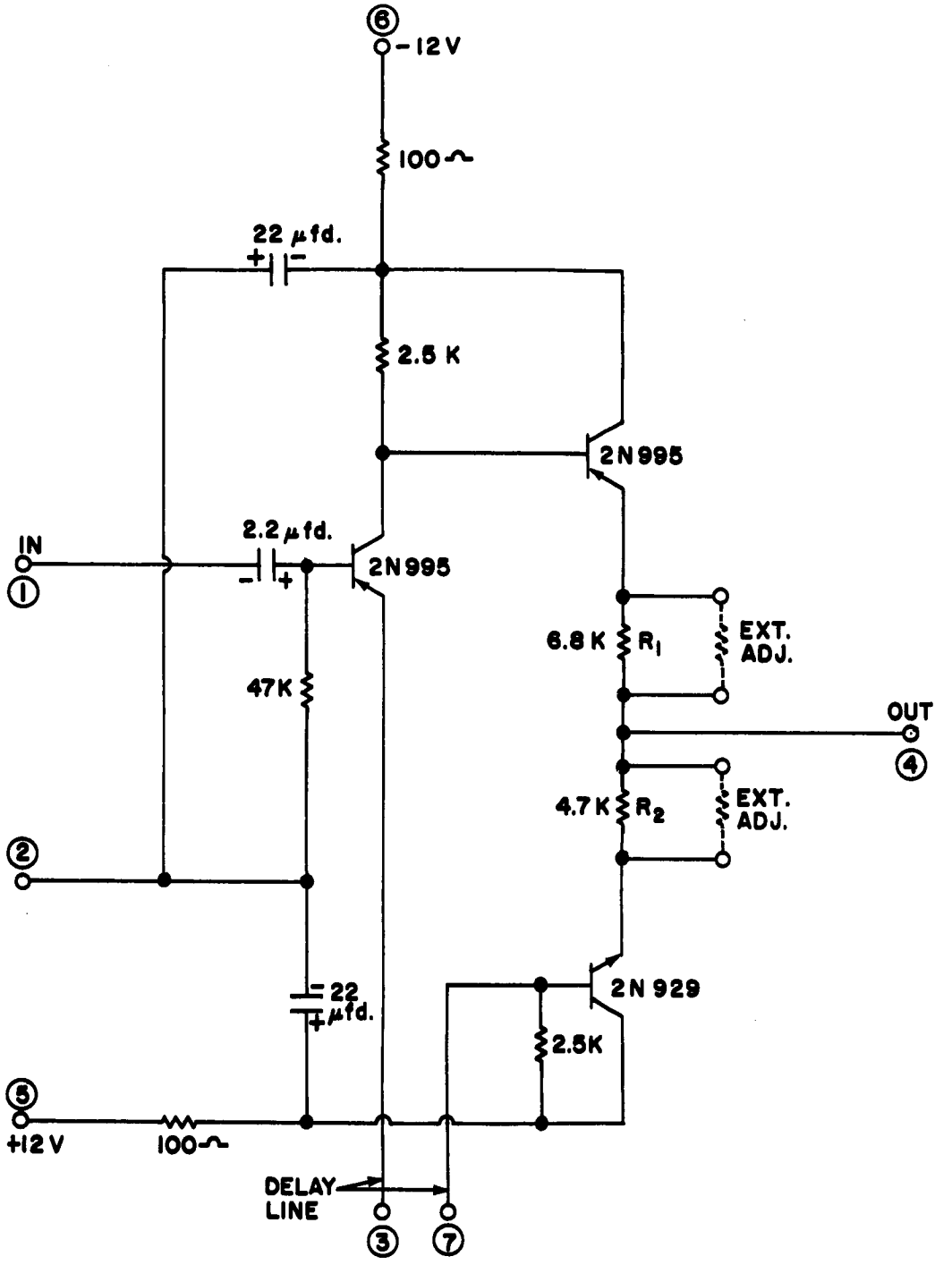


Figure 7–Shaper, Two Microsecond

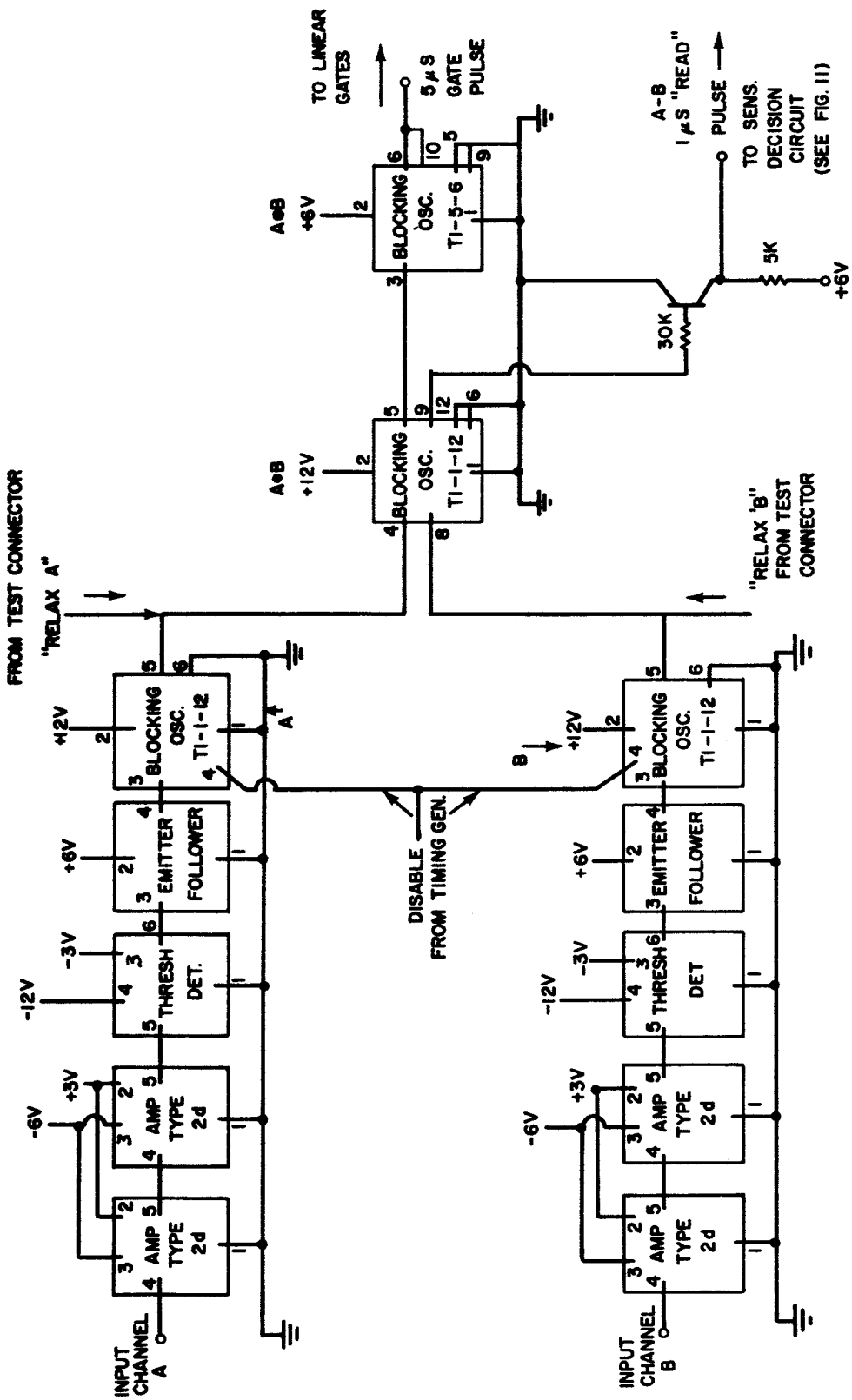


Figure 8—Interconnection of Coincidence Logic Circuits

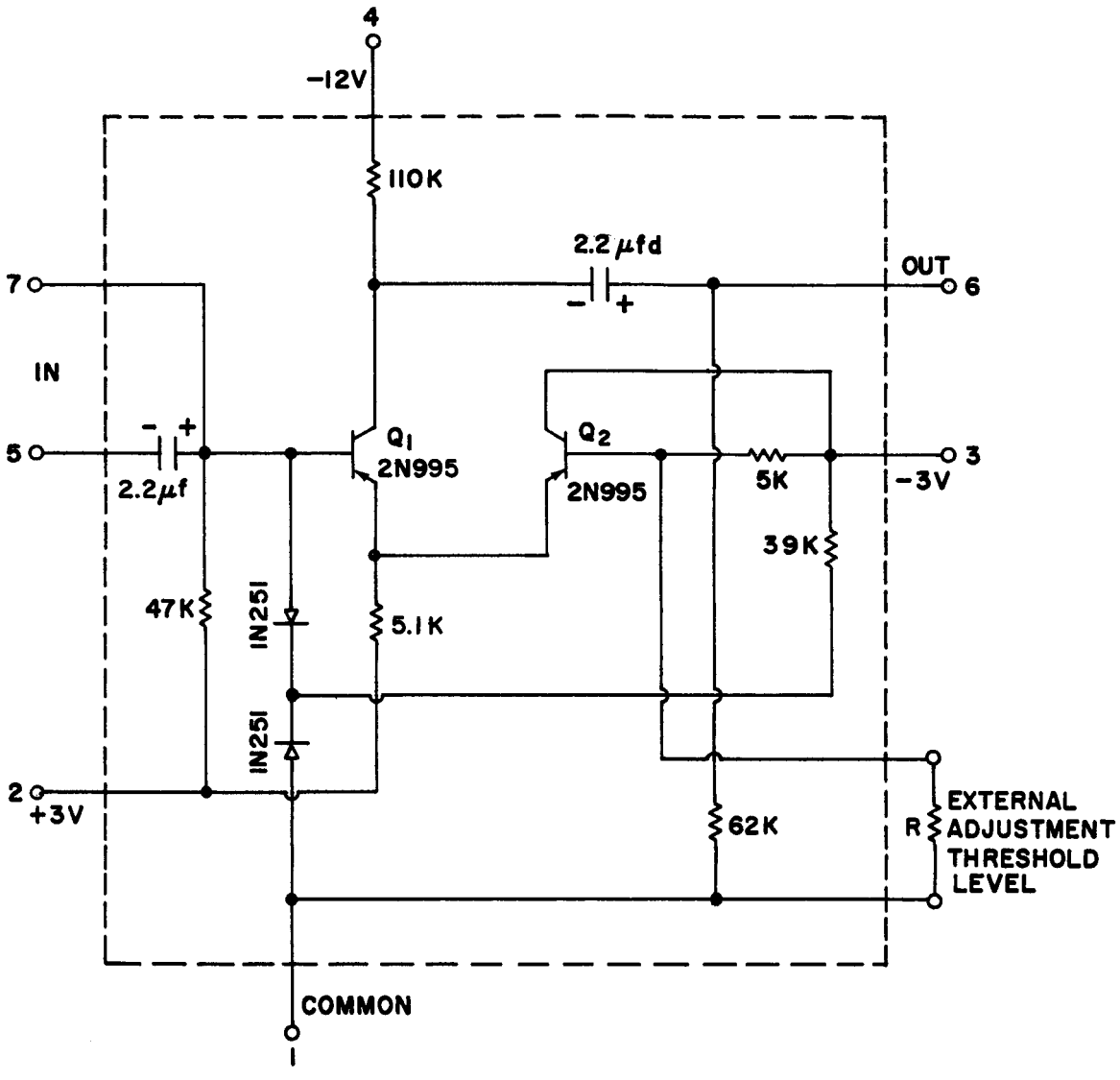


Figure 9–Threshold Detector

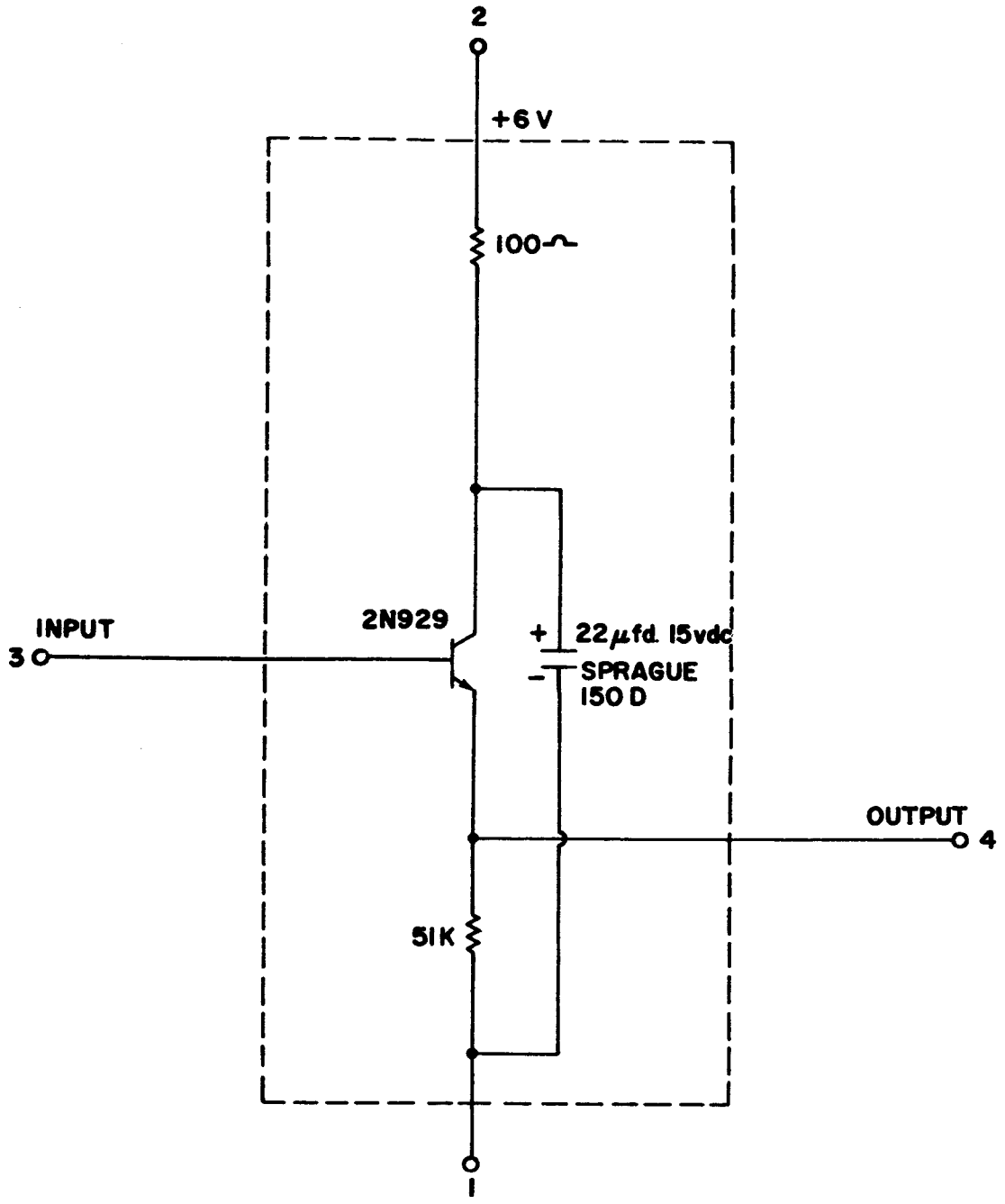


Figure 10–Emitter Follower

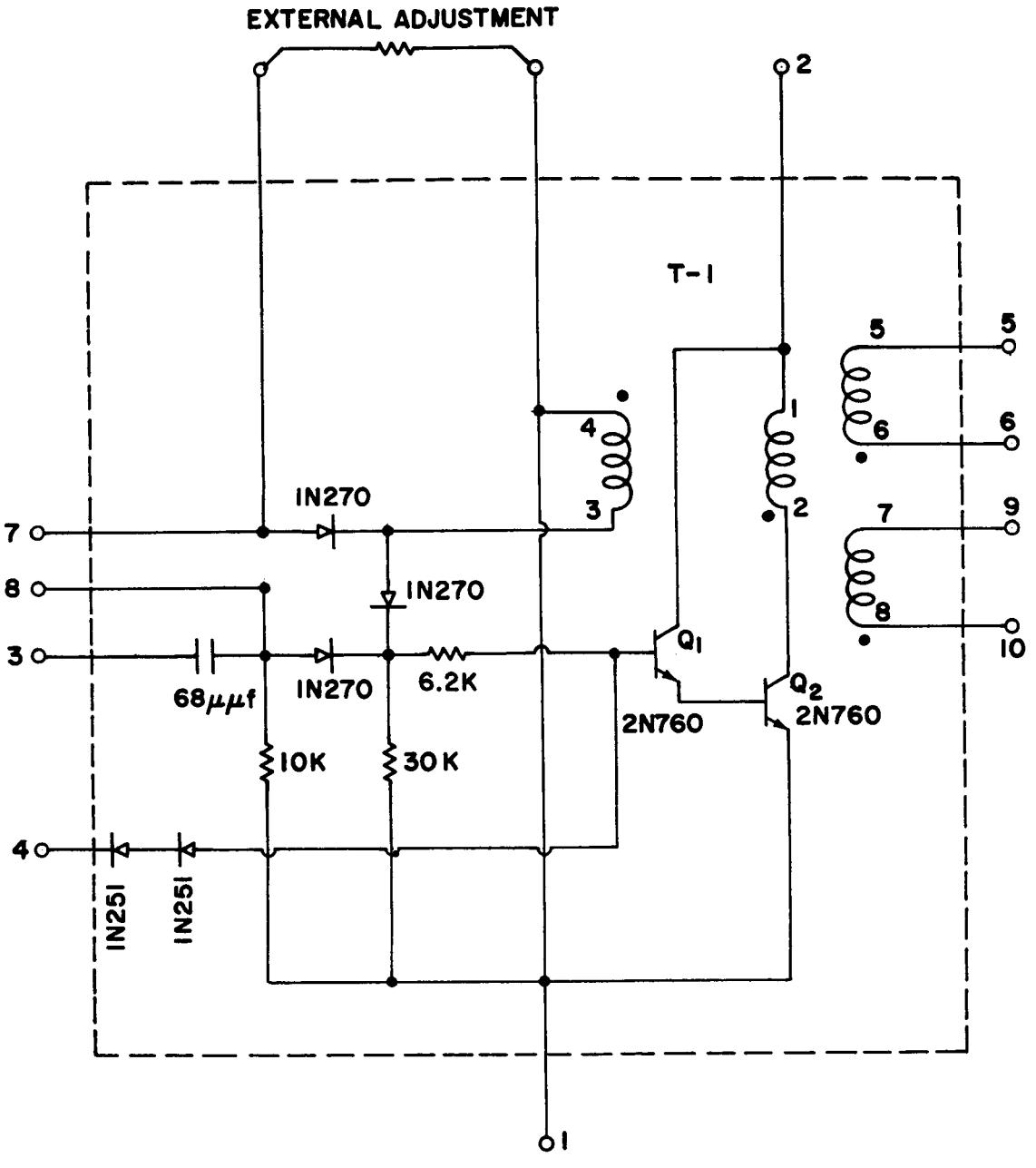


Figure 11–Blocking Oscillator BO–1-

Transformer design and corresponding output pulse width are shown in the following table.

Table 2

Pulse Width	Transformer Type No.	Alladin No.	Windings				Supply Volts
			1-2	3-4	5-6	7-8	
1 μsec	T1-1-12	01-601	13	39	13	13	12
5 μsec	T1-5-6	01-603	28	84	28	28	6

In normal operation, the A·B blocking oscillators are triggered only when a signal is present in both Channel A and Channel B. The first A·B blocking oscillator furnishes a 1 microsecond pulse to operate the sensitivity decision circuit and also to trigger the second A·B blocking oscillator. The second A·B blocking oscillator initiates action in the timing generator and furnishes a 5 microsecond pulse to operate the linear gates in channels A, B, and C. As soon as the timing generator begins operation, an inhibit signal is returned to the A blocking oscillator and to the B blocking oscillator to prevent any additional inputs from initiating coincidence circuit gating action while the desired signals are being processed.

Provision is made to relax the coincidence logic requirement under test conditions by means of the "Relax A" or "Relax B" inputs from the test connector. A D-C voltage applied to the "Relax A" input allows the A·B blocking oscillators to be triggered by a signal in Channel B only. A D-C voltage applied to the "Relax B" input allows the A·B blocking oscillators to be triggered by a signal in Channel A only.

(5) Gain Selecting System. A wide dynamic range of 6400 to 1 is achieved in each pulse height analyzer channel by means of gain selecting circuits interconnected as shown in Figure 12. These circuits are divided into the following groups:

(1) A variable-gain amplifier

(2) Threshold Detector Amplifiers

(3) Threshold Detectors

(4) Sensitivity Decision Circuit

(5) Bistables and Attenuator Switches

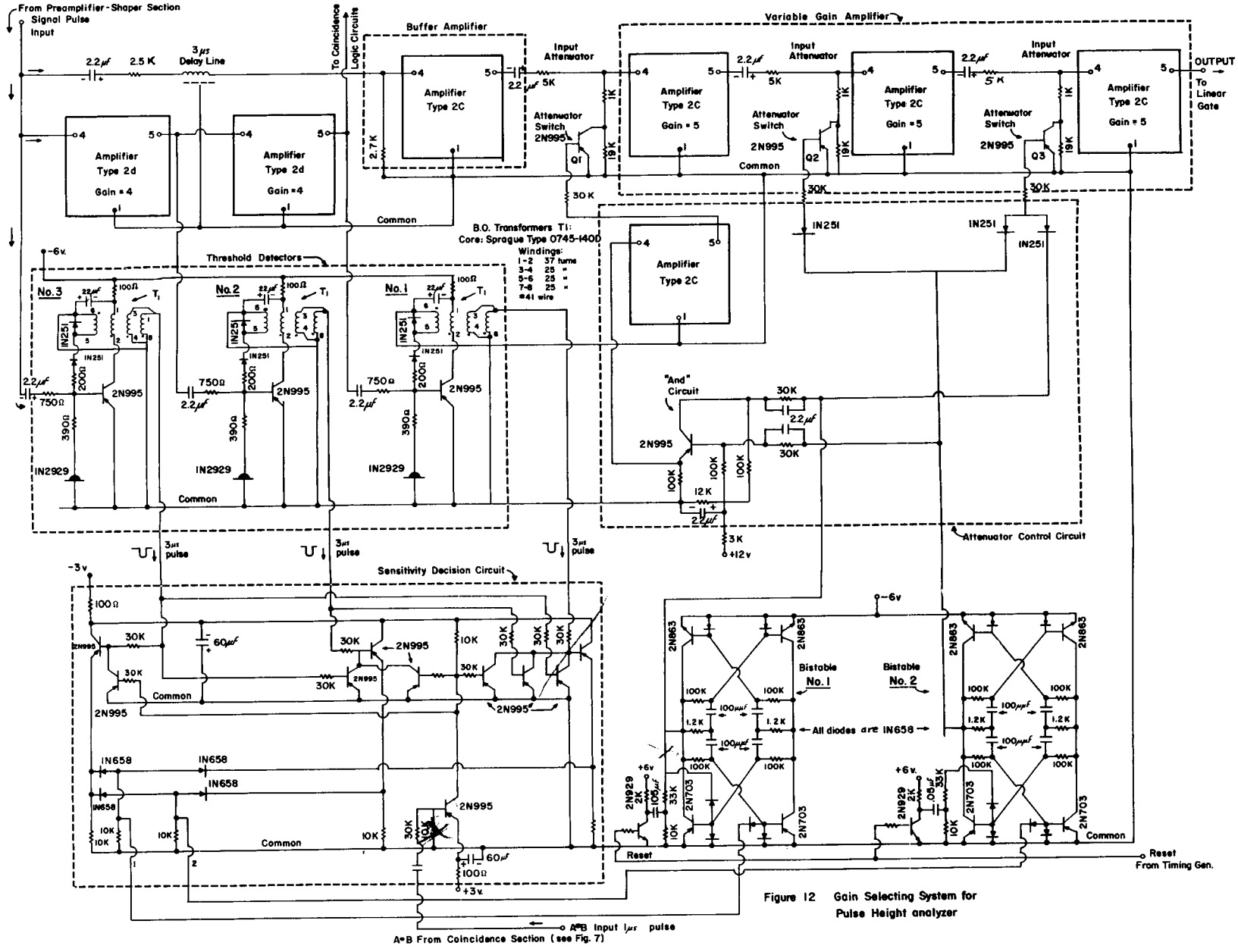


Figure 12 Gain Selecting System for Pulse Height analyzer

Each negative-going signal pulse from the preamplifier-shaper section is fed to the variable-gain amplifier through a 3 microsecond delay line and buffer amplifier. The delay is included to allow time for the coincidence logic and sensitivity decision circuits to operate before the signal passes through the variable-gain amplifier to the linear gate. The signal pulse is also applied to the first threshold detector amplifier (type 2d) and to Threshold Detector No. 3.

The variable-gain amplifier consists of three amplifiers type 2c, each with a gain of 5, and each preceded by a transistor-switched attenuator. Each attenuator switch controls the net gain of the amplifier and attenuator as indicated in Table 3.

Table 3
Variable Gain Operation

Attenuator Switch	Effective Attenuation	Net Stage Gain
Off	4/5	$4/5 \times 5 = 4$
On	1/5	$1/5 \times 5 = 1$

The on-off condition of the three attenuator switches (Q1, Q2 and Q3) is determined by the condition of the two bistables. This, in turn, determines the over-all gain of the variable-gain amplifier. A "reset" pulse from the timing generator at the end of each scaling and readout action places both bistables in their initial condition "0". The bistables remain at "0" or are changed to "1" by the action of the sensitivity decision circuit in response to input signals.

A signal pulse below 80 mv (at the input to the preamplifier-shaper section) does not trigger any of the threshold detectors and there is no output from the sensitivity decision circuit. Both bistables remain at "0" and the overall gain of the variable-gain amplifier is 64.

A signal pulse between 80 mv and 320 mv is amplified by the threshold detector amplifiers (type 2d) sufficiently to trigger Threshold Detector No. 1. This circuit furnishes a 3 microsecond pulse to the sensitivity decision circuit which in turn switches bistable No. 1 to "1" when the coincidence circuit $A \cdot B$ signal arrives. Overall gain of the variable gain amplifier for input signals between 80 mv and 320 mv is 16.

An input signal between 320 mv and 1.28 v is amplified by the threshold detector amplifiers sufficiently to trigger Threshold Detector No. 1 and No. 2. These circuits each furnish a 3 microsecond pulse to the sensitivity decision circuit which in turn switches bistable No. 2 to "1" and leaves bistable No. 1 at "0". Overall gain of the variable-gain amplifier for input signals between 320 mv and 1.28 v is 4.

An input signal greater than 1.28 v triggers all three threshold detectors. The three threshold detector outputs to the sensitivity decision circuit switches both bistables to "1". The overall gain of the variable-gain amplifier for input signals greater than 1.28 v is 1.

Operation of the gain selecting system is summarized in Table 4.

Table 4
Operation of Gain Selecting System

Input Signal to Preamplifier-Shaper Section	Threshold Detector Outputs			Bistables		Attenuator Switches			Overall Gain
	No. 1	No. 2	No. 3	No. 1	No. 2	Q1	Q2	Q3	
Less than 80 mv	0	0	0	0	0	off	off	off	64
80 mv to 320 mv	0	0	1	1	0	off	off	on	16
320 mv to 1.28 v	0	1	1	0	1	off	on	on	4
Greater than 1.28 v	1	1	1	1	1	on	on	on	1

It should be pointed out that no attenuator switching action takes place for signals in the lowest range, hence there is no problem of switching transients when the system is at maximum gain.

(6) Linear Gate, Figure 13. Transistors Q1 and Q2 are normally OFF and conduct only when a gating pulse from the coincidence logic circuits is present on the secondary winding of the pulse transformer. Voltage drop from the Q1 emitter to the Q2 emitter is negligible compared to 10 mv. The parallel combination of diode, resistor, and capacitor in the transistor base circuits is necessary to minimize transients in the gated output due to the rise and fall of the gating pulse.

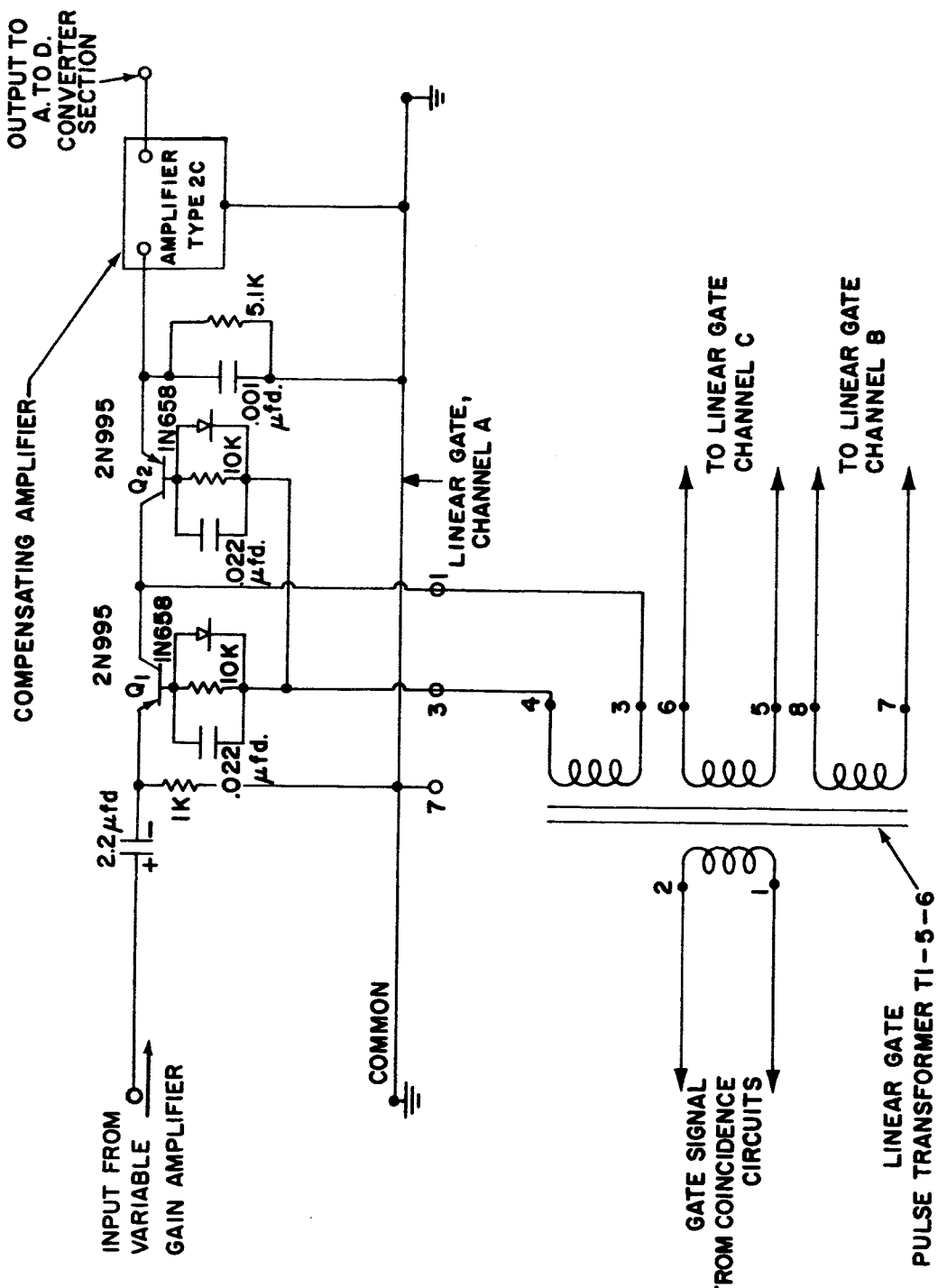


Figure 13–Linear Gate

A negative-going signal pulse from the variable-gain amplifier is applied to Q1 emitter. When Q1 and Q2 are conducting, this signal is fed to the compensating amplifier type 2c and then to the A. to D. Converter section.

(7) A. to D. Converter Section. The analog to digital converter section in each pulse height analyzer channel consists of the following circuits:

Sweep Circuit, Figure 14
Sweep Control, Figure 15
Output Shaper, Figure 16
Output Gate, Figure 17

These circuits operate in conjunction with the following circuits which are common to all three pulse height analyzer channels:

Busy Bistable, Figure 18
Trigger Delay, Figure 19
500 kc Clock, Figure 20

Interconnection of the A. to D. converter circuits for all three pulse height analyzer channels and the circuits common to all channels is shown in the schematic of Circuit Board No. 2, Figure 31. Operation is illustrated by the waveforms in Figure 2. A negative-going input signal to the sweep circuit is amplified by Q1 and Q4. This charges the capacitor C1 and C2 to a negative value proportional to signal peak amplitude. This potential remains at the peak level as long as Q5 is non-conducting. Emitter followers Q3 and Q2 transfer the capacitor voltage to Q1 emitter, thus the net drive on Q1 is the difference between input signal amplitude and negative emitter voltage. The positive-going portion of the input signal causes Q1 to conduct and feeds a positive pulse through Q4 to the output shaper to initiate a positive shaper signal. After a 4 microsecond delay to insure that the capacitors charge to the full negative signal peak, coincidence between shaper output and a clock pulse places the busy bistable in the SET condition. The busy bistable SET signal causes Q5 to conduct, and the combination of Q5 and the 6.2 volt zener diode (T1653CO) acting as a constant current source discharges C1 and C2 at a constant rate. This discharge begins at the leading edge of the busy bistable signal F and ends when the capacitor voltage drops to its quiescent value. At this point Q1 stops conducting and a negative-going signal from Q1 through Q4 terminates the positive shaper signal.

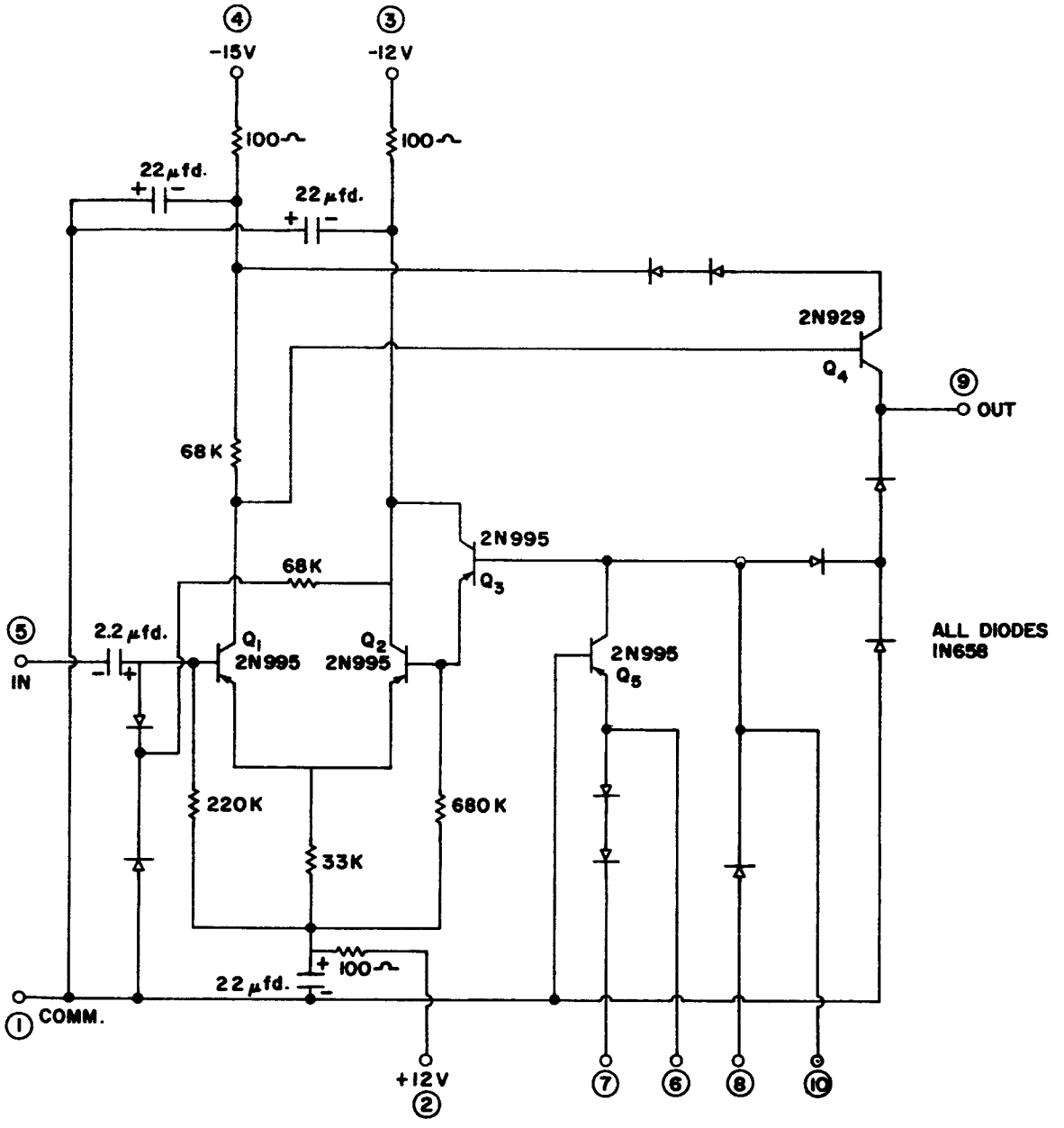


Figure 14–Sweep Circuit

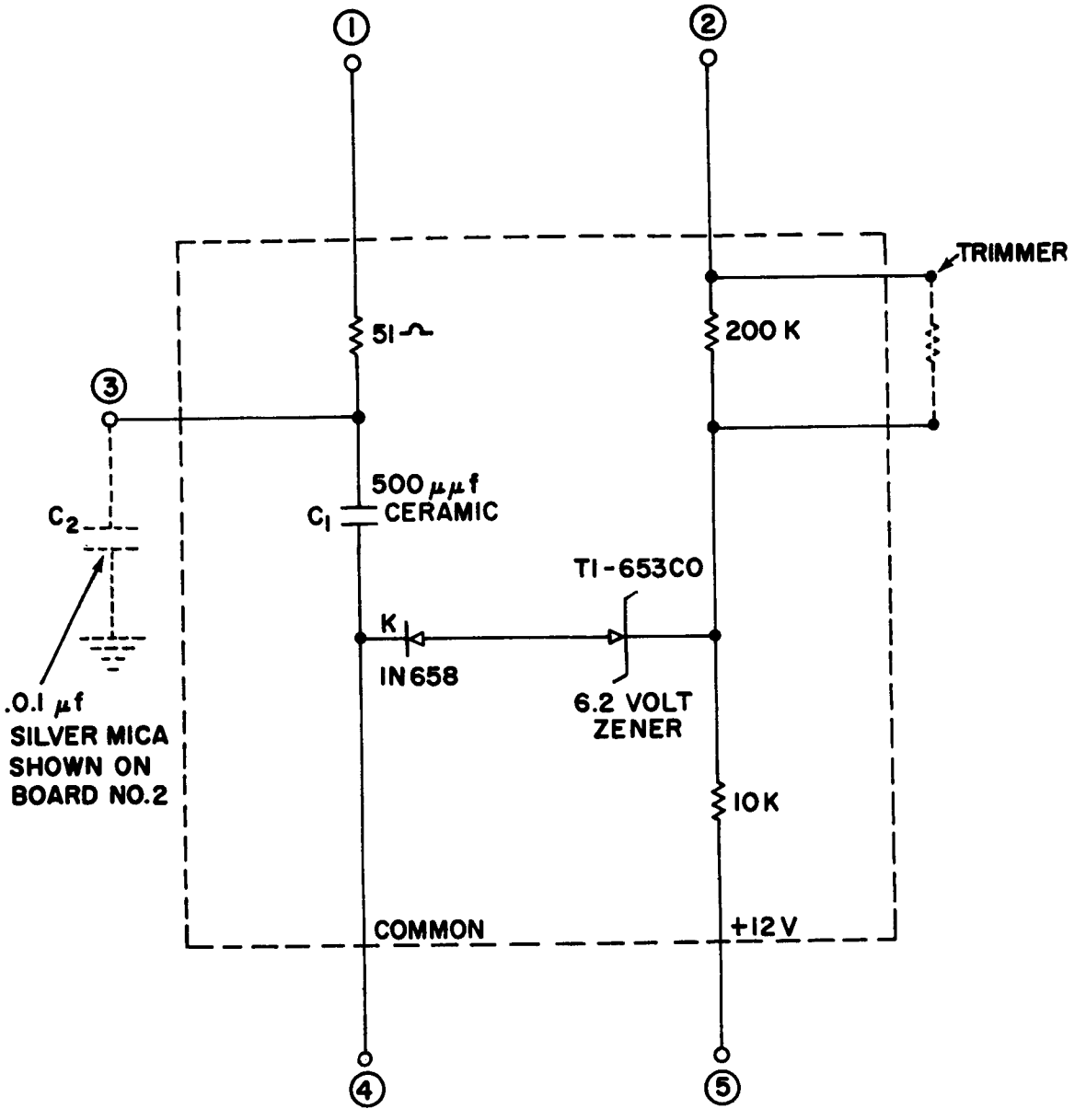


Figure 15–Sweep Control

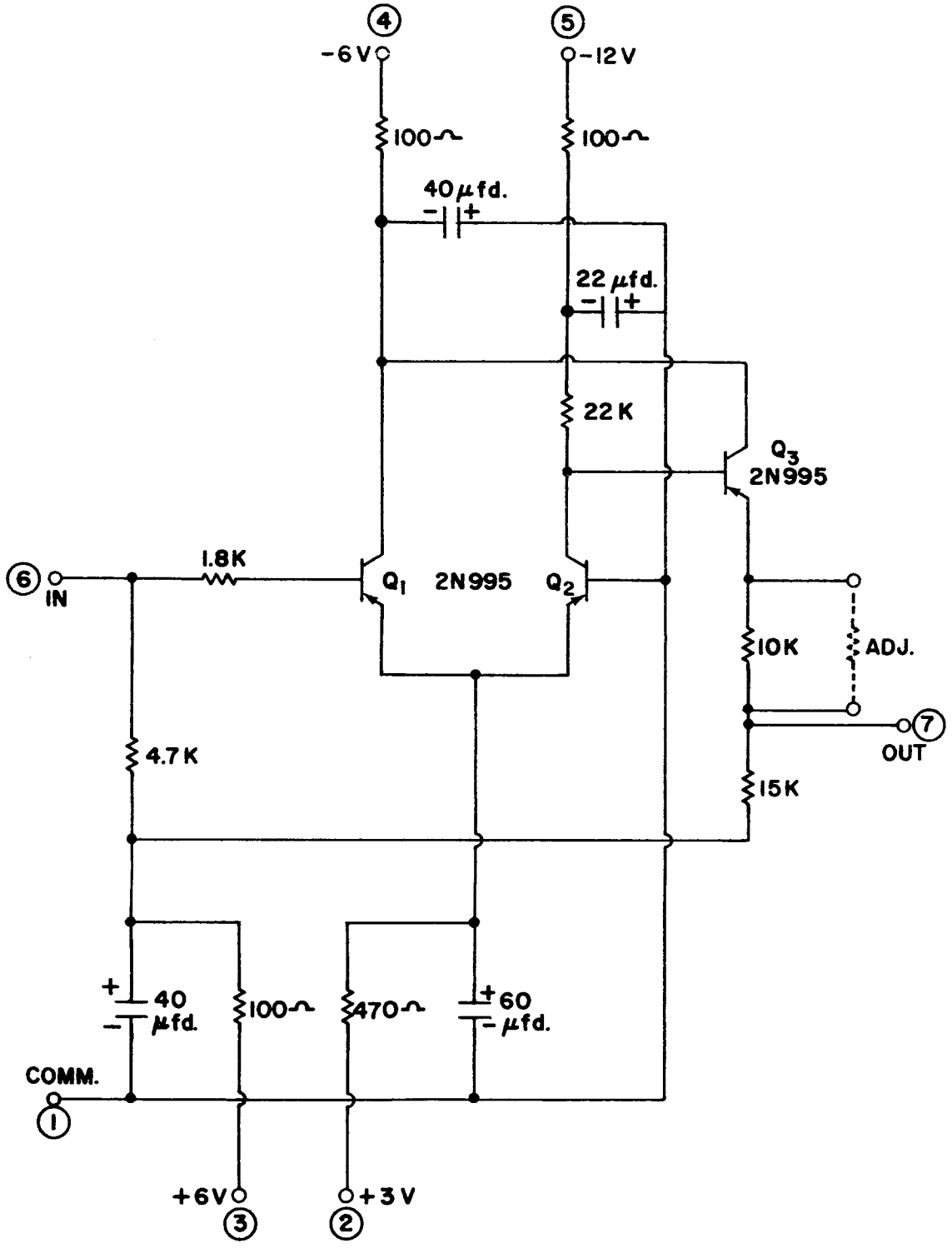


Figure 16–Output Shaper

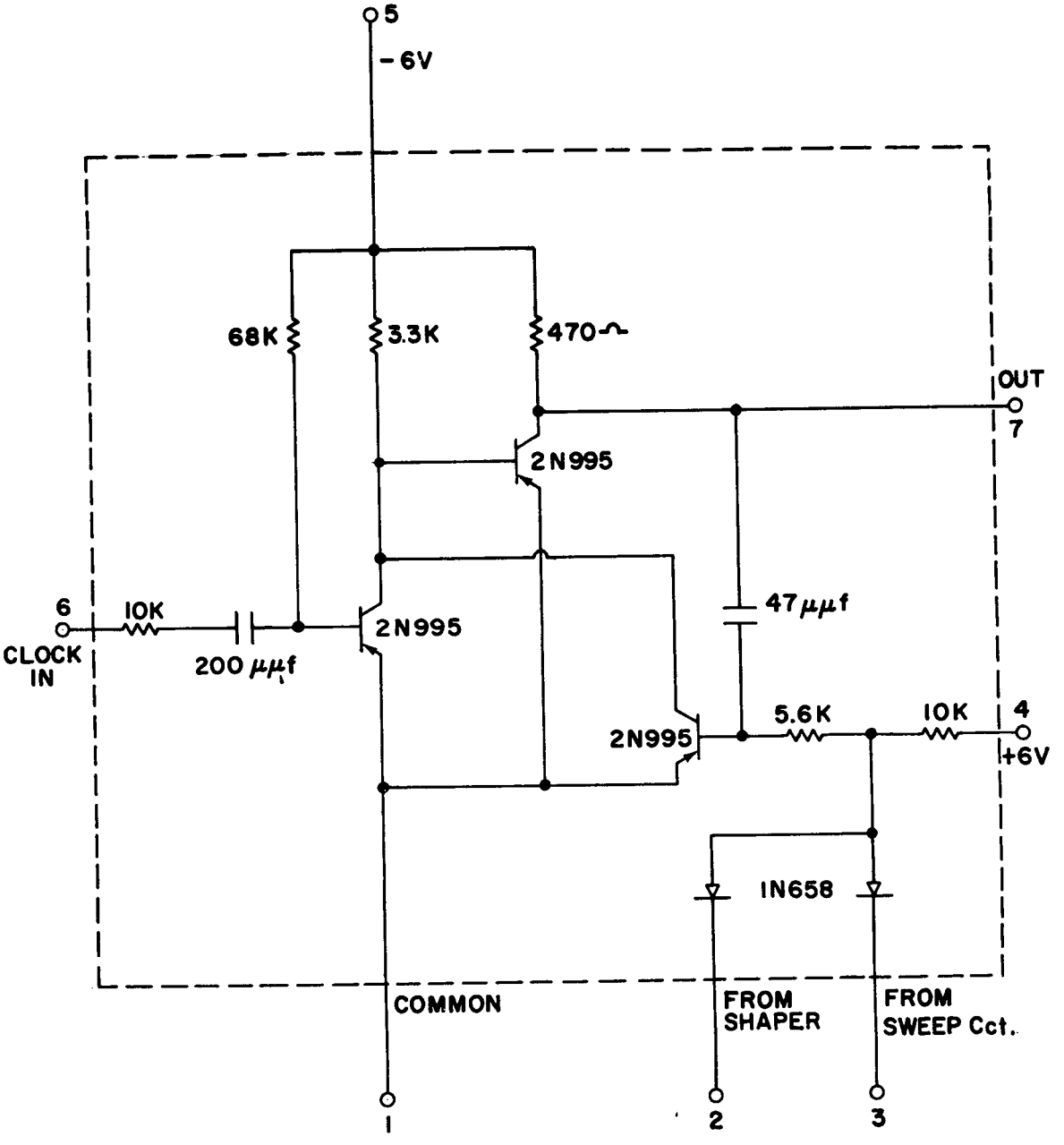


Figure 17–Output Gate

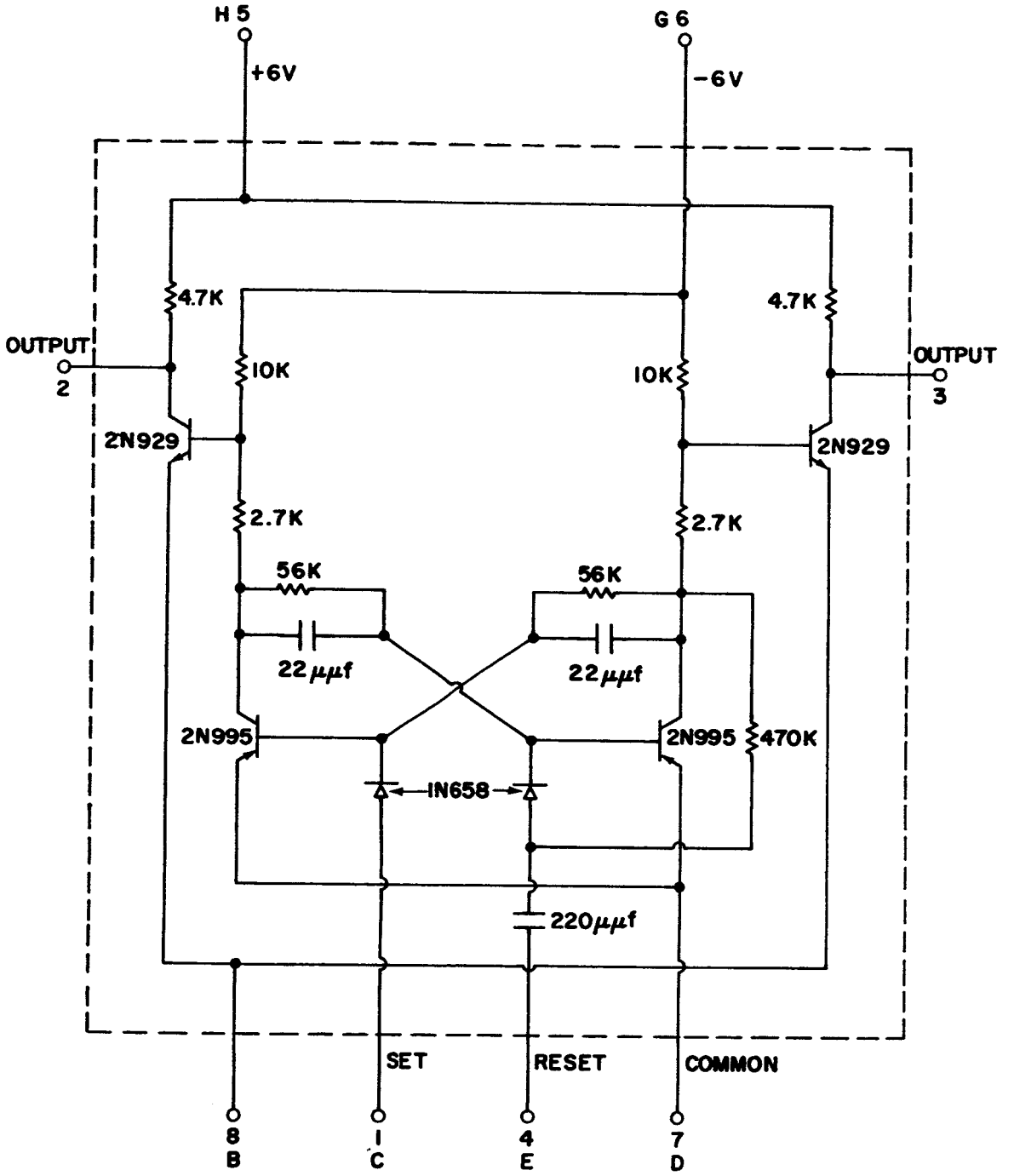


Figure 18–Busy Bistable

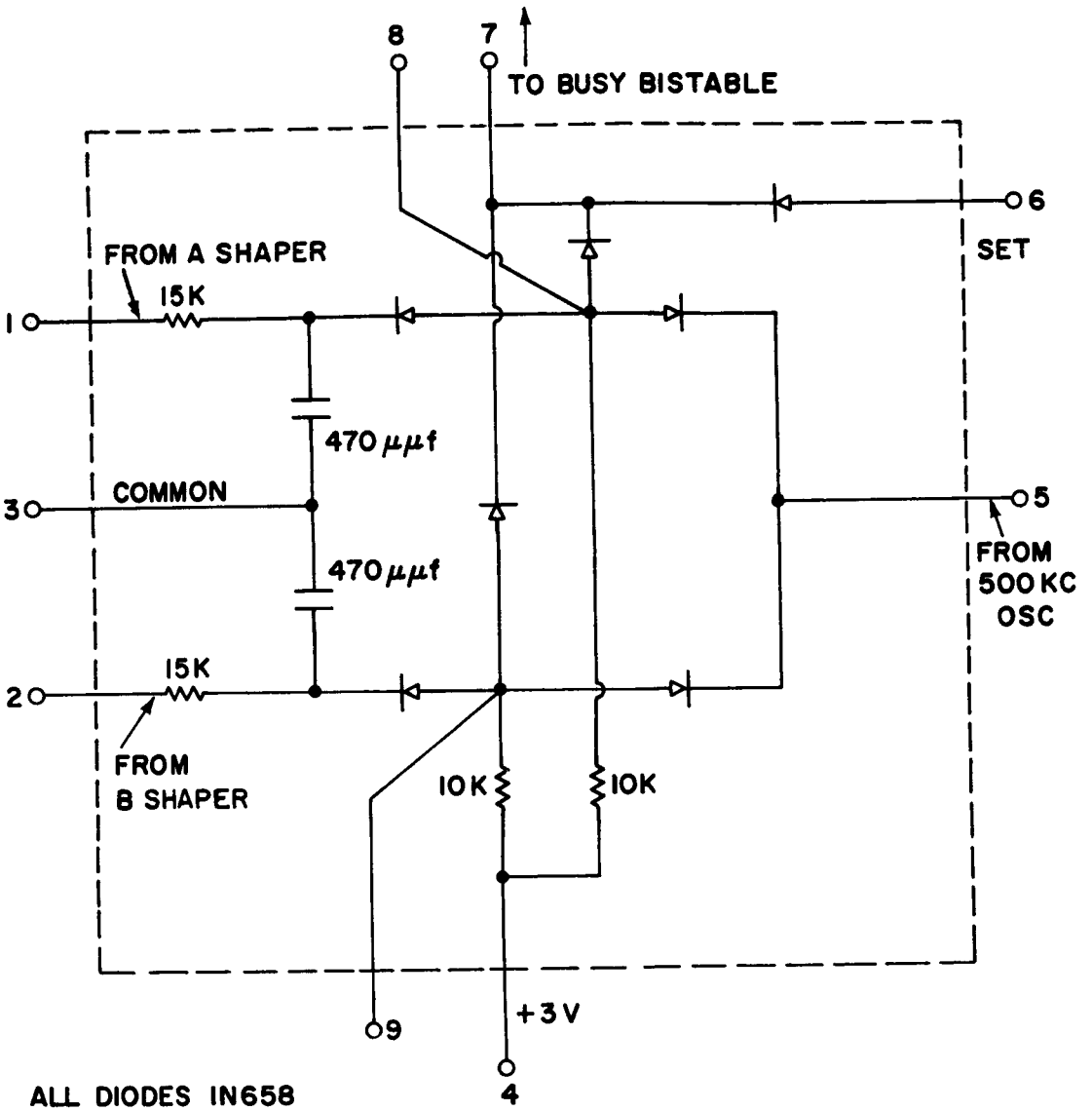


Figure 19–Trigger Delay

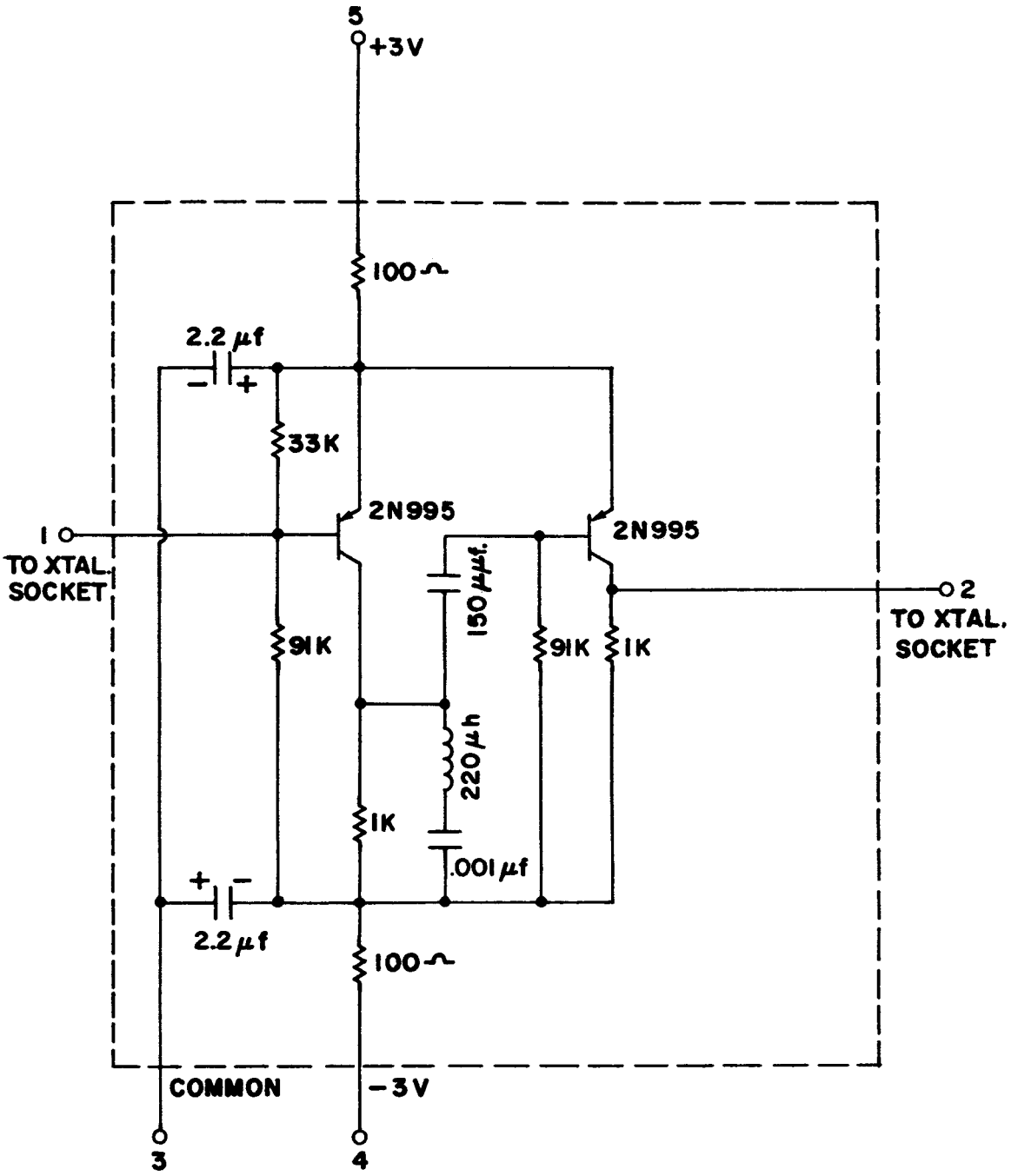


Figure 20–500 kc Clock

The output gate is normally blocked, and becomes unblocked only during coincidence of the positive shaper output and the busy bistable SET signal. This coincidence endures as long as capacitors C1 and C2 are discharging, which depends on the voltage to which they are initially charged. Thus, the number of 500 kc oscillator pulses which pass through the output gate is proportional to the input signal amplitude. The circuit is designed to generate a 2 microsecond gate in response to a 10 millivolt signal applied to the sweep circuit input, and is linear for input signals up to 5.12 volts.

The busy bistable is normally in the RESET condition, which allows a scaling and readout action to take place whenever there is coincidence of signals in channels A and B. The bistable is placed in the SET condition whenever there is coincidence of a 500 kc clock pulse and a shaper pulse. The Trigger Delay logic circuit, Figure 23, furnishes the SET trigger pulse approximately 4 μsec. after coincidence of the clock and shaper pulses. The 4 μsec delay is obtained from the 15K and 470$\mu\mu$f networks in the Trigger Delay Circuit.

The 500 kc clock is a crystal controlled oscillator with emitter follower output.

Digital Data Circuits

(1) Scaler, Figure 21. Component values depend on the location of the scaler in the system as indicated on the schematic.

(2) Readout Switch, Figure 22. Each readout switch is a transistor driver with an "AND-OR" input logic. Output pulse to recorder head, 2 to 3 ma., 2 ms duration.

Scaling and Readout Timing Generator

Schematics for the two monostable multivibrators comprising the timing generator are shown in Figure 23 and Figure 24. Transformer design data is as follows:

Core: Magnetics, Inc. 50033-1A tape-wound "square loop" toroid.

1-2	1350 turns	9-10	300 turns
3-4	198 turns	11-12	400 turns
5-6	1350 turns	13-14	1750 turns
7-8	198 turns	15-16	300 turns

	STAGE I	STAGES 2-9	TIMER SCALERS
R_1	220K	150K	220K
R_2	300Ω	600Ω	300Ω
R_3	1.5K	3K	1.5K
C_1, C_2	150pf.	47pf	47pf

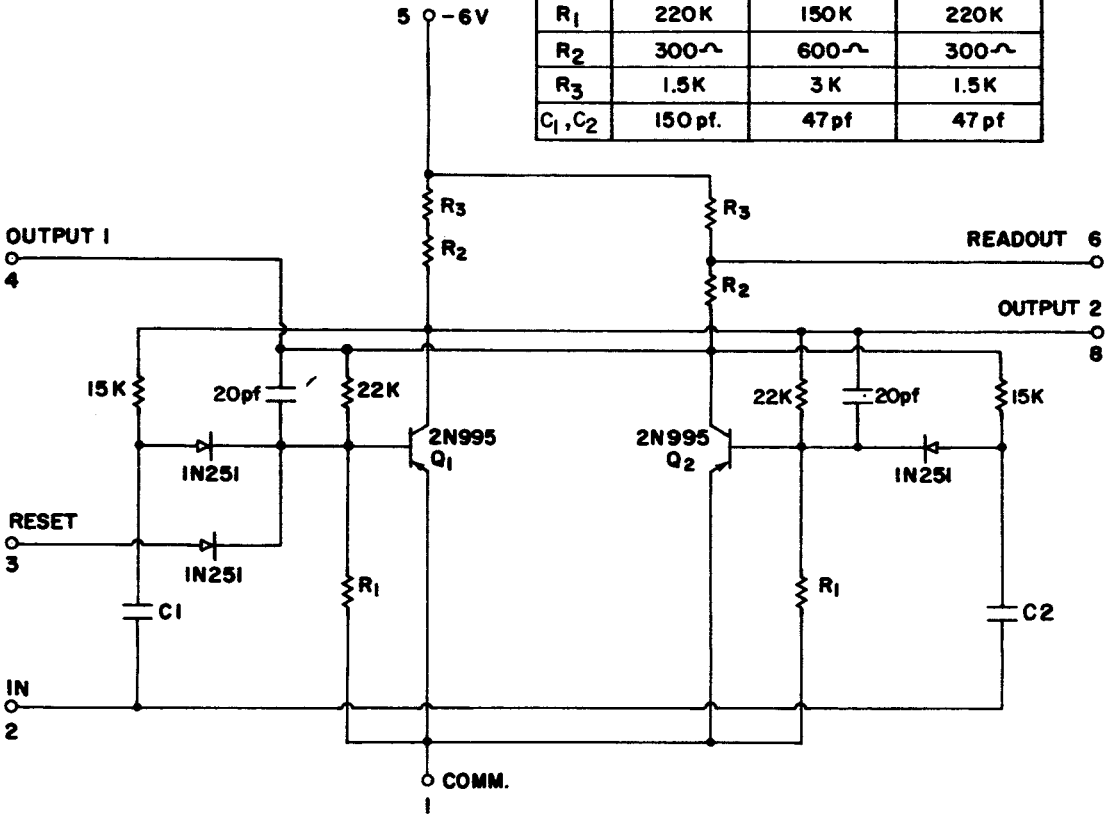


Figure 21–Scaler

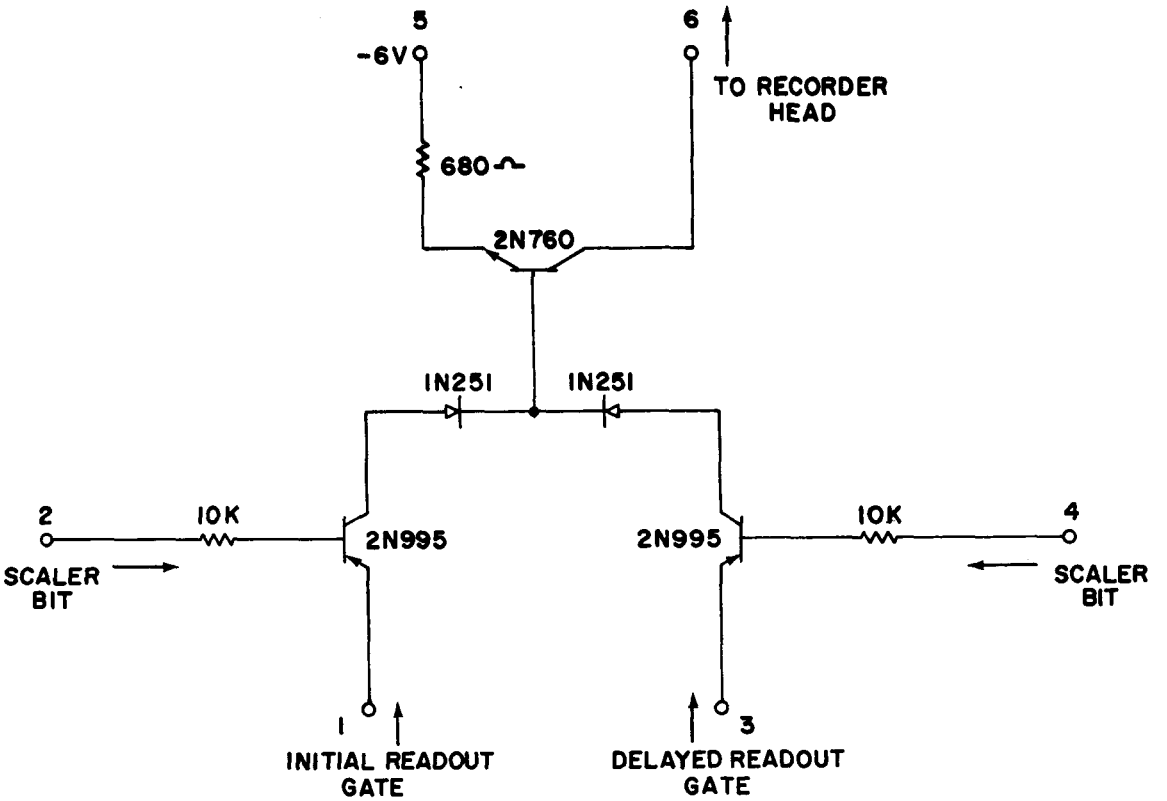


Figure 22–Readout Switch

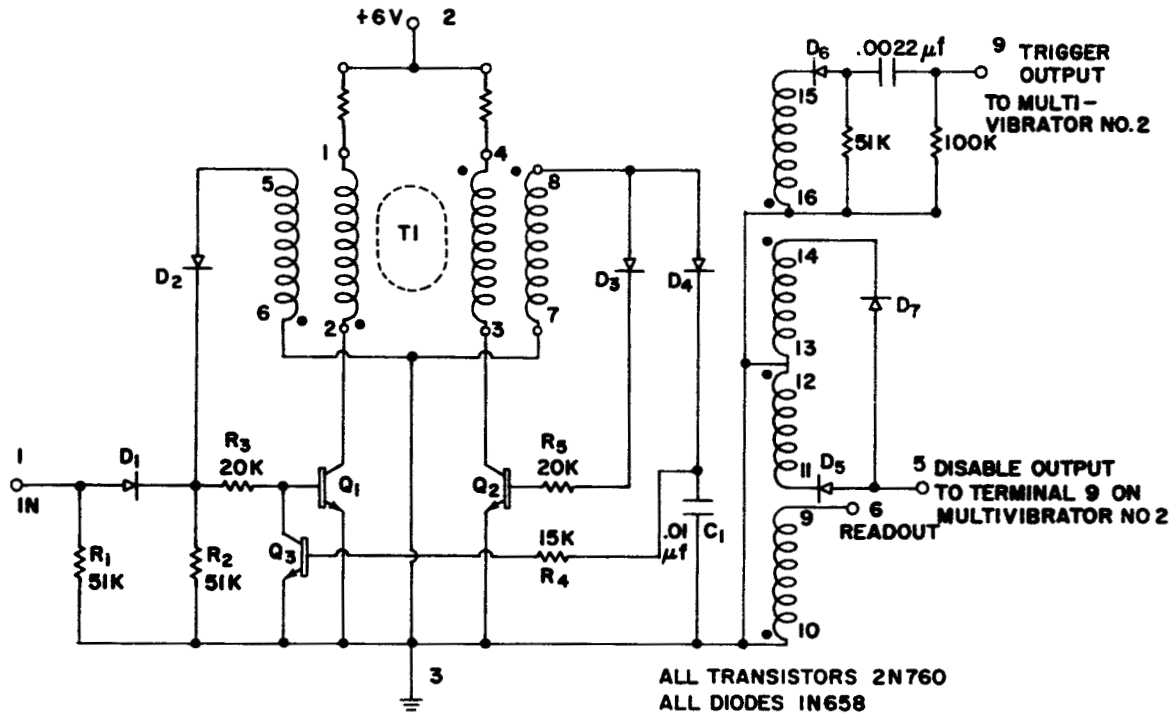


Figure 23–Timing Generator Multivibrator No. 1

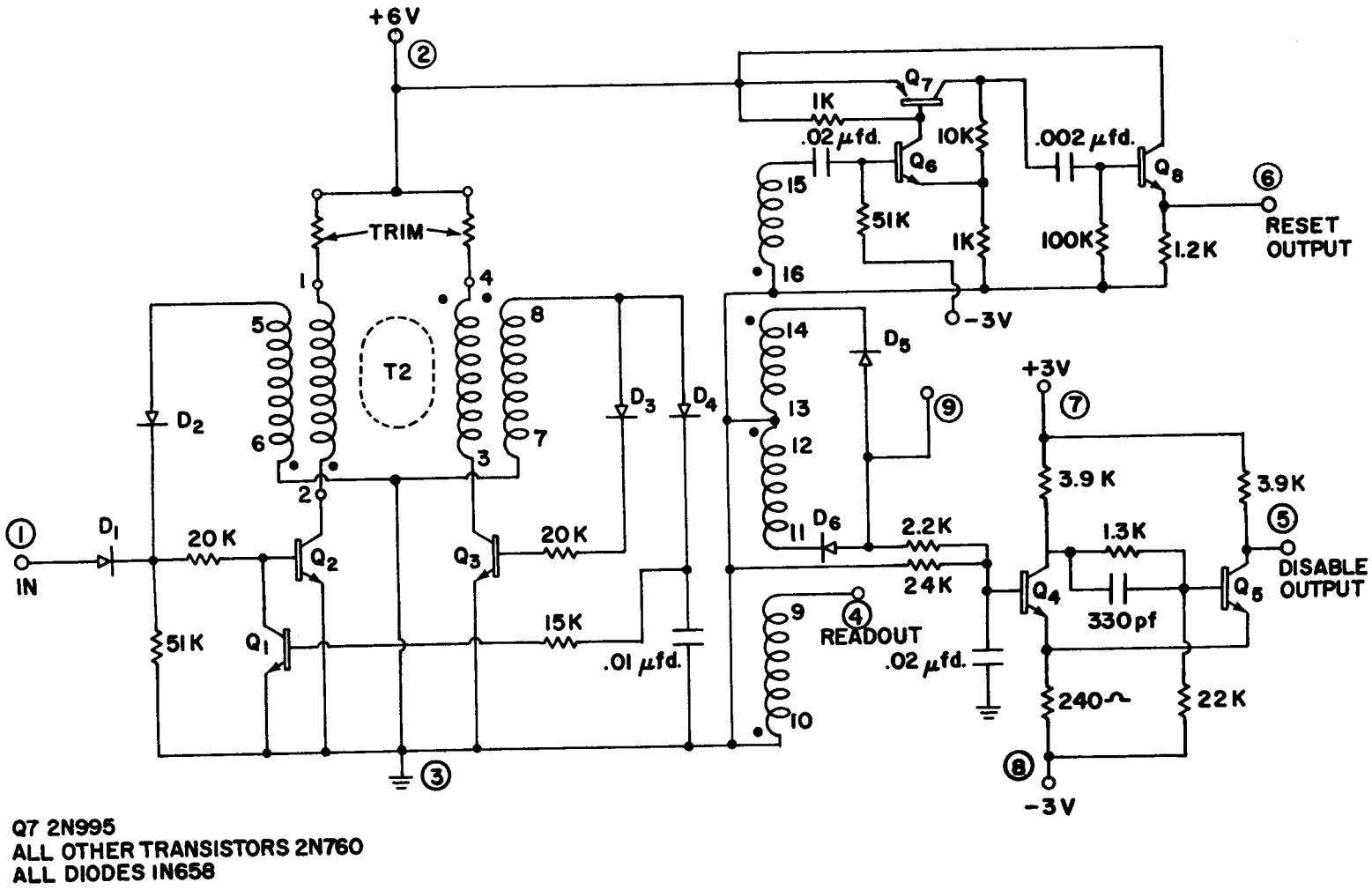


Figure 24—Timing Generator Multivibrator No. 2

Power Supply and Heater Circuits

(1) Battery and Power Converter, Figure 25. Power for the entire system is obtained from a battery of sixteen silver cells, Yardney type HR-10. Eight of these cells connected in series furnish 12 volts for the heater. The remaining eight cells are connected in series to furnish +6 volts and -6 volts with respect to circuit common.

The power converter is an Astronetics type PS-24 operating on 12 volts input. Converter output to the electronics is ∓12 volts, ∓3 volts and -15 volts. A portion of the +6 volt and -6 volt battery load also goes to the electronics. An arming plug is provided to energize all circuits when it is inserted into connector S-16.

Load currents and power have been measured under standby conditions and under two different operating conditions described as follows:

(a) Maximum Coincident Event Rate. In this condition coincident events in channels A, B, and C are being processed at 35 events per second. This is approximately the maximum operating speed as determined by the scaling and readout timing generator. Current and power data under this condition are tabulated under "Coincidence Operation, 35 cps."

(b) Maximum Non-coincident Operation. In this condition, non-coincident events operating in one of the three channels at 85 kc to 125 kc causes "worst case" power drain from the +12 volt line supplying the blocking oscillators. Current and power data under this condition are tabulated under "non-coincident operation, 85 kc."

Table 5 gives load current and power drain for the electronics battery (excluding heater power) and for the various d-c voltage lines to the electronics circuits. These figures show overall power consumption and also may be useful in locating circuit malfunctions.

(2) Heating and Heater Control Circuit, Figure 26. The heater is controlled by a proportional ON-OFF circuit with thermistors and transistors operating a heating element from a separate 12 volt battery. The heating element consists of 20 feet of number 31 wire fastened to the electronics rack. In the OFF condition the control circuit draws 2.1 milliamperes. In the ON condition the heater draws 2.8 amperes. The control circuit is expected to keep the heating element turned off at all temperatures above +15°C.

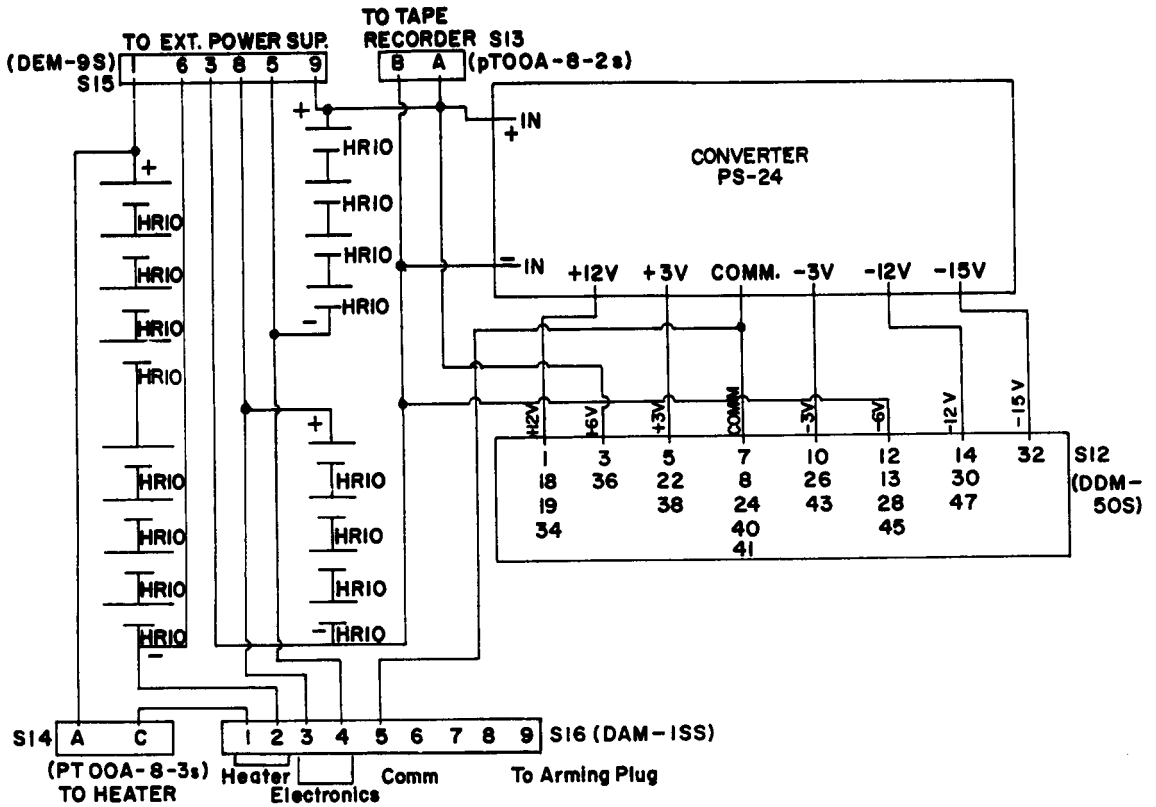


Figure 25–Battery and Power Converter

Table 5
Electronics Circuits Current and Power Drain

Circuit	Standby Operation		Coincidence Operation 35 cps		Non-Coincidence Operation 85 kc	
	Current, ma	Power, mw	Current, ma	Power, mw	Current, ma	Power, mw
Total Battery, +6 v	87	522	90	540	108	648
Total Battery, -6 v	140	840	144	864	185	1110
+6 v to Electronics	10	60	12	72	12	72
-6 v to Electronics	63	78	66	396	89	534
Converter, Input +6 v	77	462	78	468	96	576
Converter, Input -6 v	77	462	78	468	96	576
Total Converter in.		924		936		1152
Converter Output						
+12 v	22	264	22	264	28	336
+3 v	21	63	21	63	22	66
-3 v	11	33	11	33	11	33
-12 v	20	240	20	240	20	240
-15 v	4	60	5	75	5	75
Total Converter out.		660		675		750

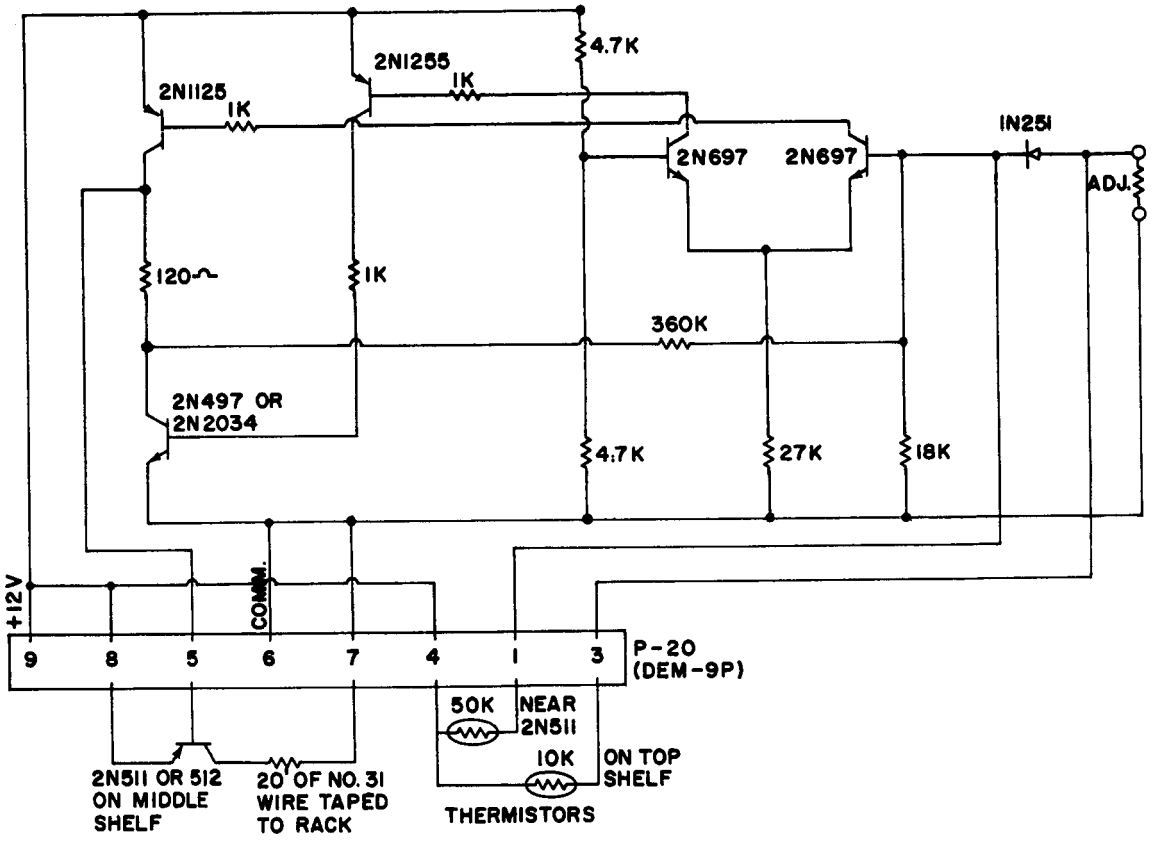


Figure 26–Heater and Temperature Control Board

CIRCUIT BOARDS AND INTERCONNECTIONS

The electronics portion of the ADCR Mark 6 system is mounted on six printed circuit boards interconnected by a single cable harness.

Board No. 1. Interconnection of circuits on this board is shown in Figure 27. These circuits include the following:

Preamplifier-Shaper Section, Channels A, B, and C
Variable-Gain Amplifiers, Channels A, B, and C
Threshold Detector Amplifiers, Channels A, B, and C

Schematics of the circuits on this board are the following:

Amplifier Type 1b, Figure 4
Amplifier, Type 2c and 2d, Figure 5
Shaper, 2 microsecond, Figure 7
Delay Line Coupler, Figure 28
Attenuator-Amplifier, Figure 29
Attenuation Control Circuit, Figure 30

Board No. 2. Interconnection of circuits on this board is shown in Figure 31. These circuits include the following:

Threshold Detector, Figure 9
Emitter Follower, Figure 10
Blocking Oscillator, Figure 11
Sweep Circuit, Figure 14
Sweep Control, Figure 15
Output Shaper, Figure 16
Output Gate, Figure 17
Busy Bistable, Figure 18
Trigger Delay, Figure 19
500 kc Clock, Figure 20

Board No. 3. Interconnection of Circuits on this board is shown in Figure 32. These circuits include the following:

7-bit scaler, Channel A
7-bit scaler, Channel B
9 readout switches

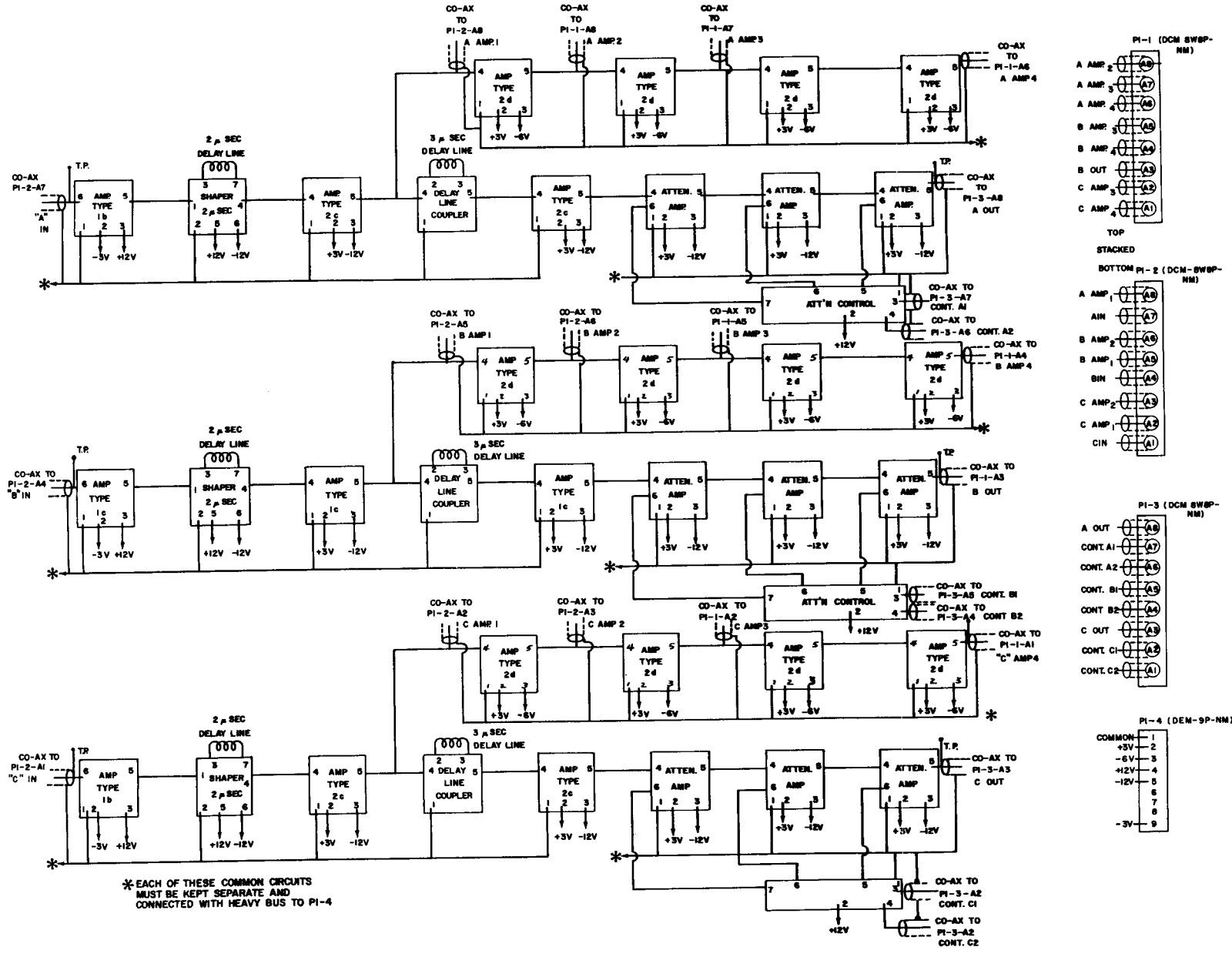


Figure 27–ADCR Mark 6 Board No. 1

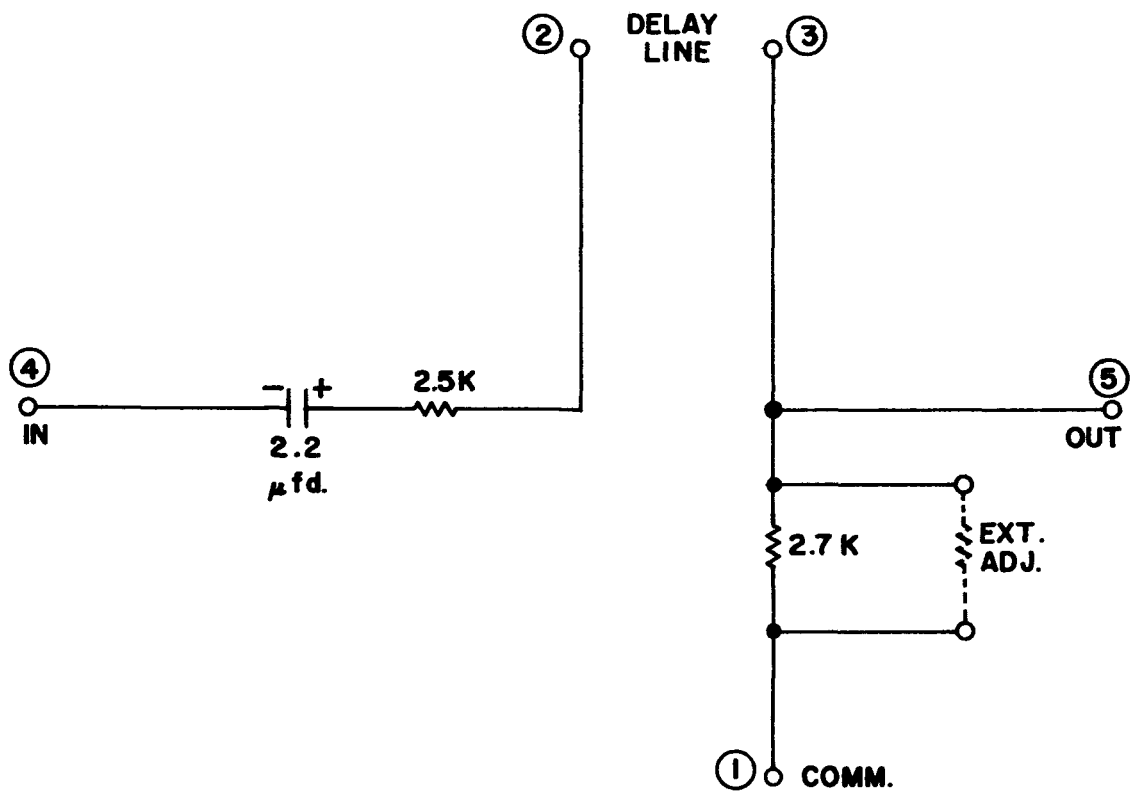


Figure 28–Delay Line Coupler

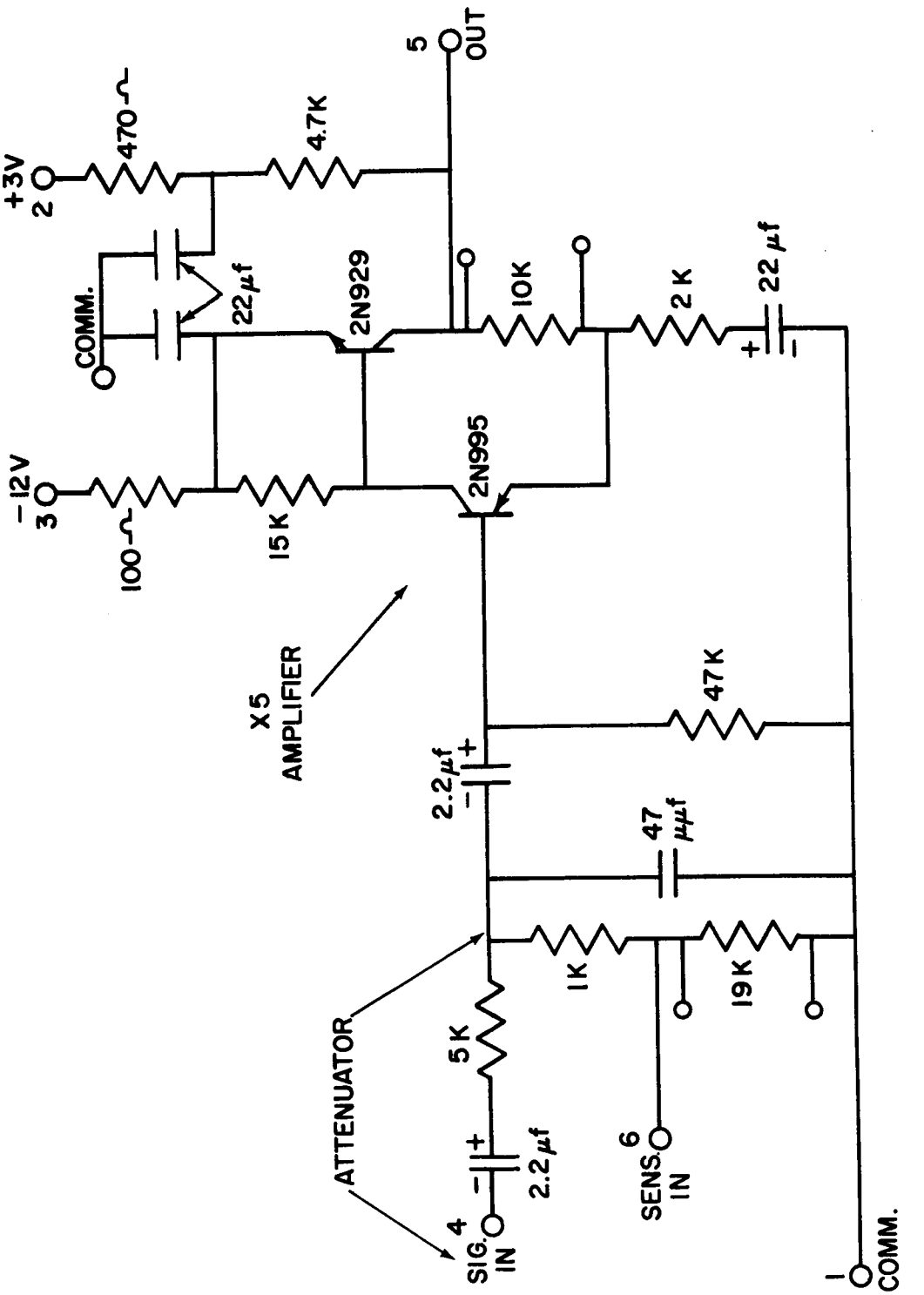


Figure 29–Attenuator-Amplifier

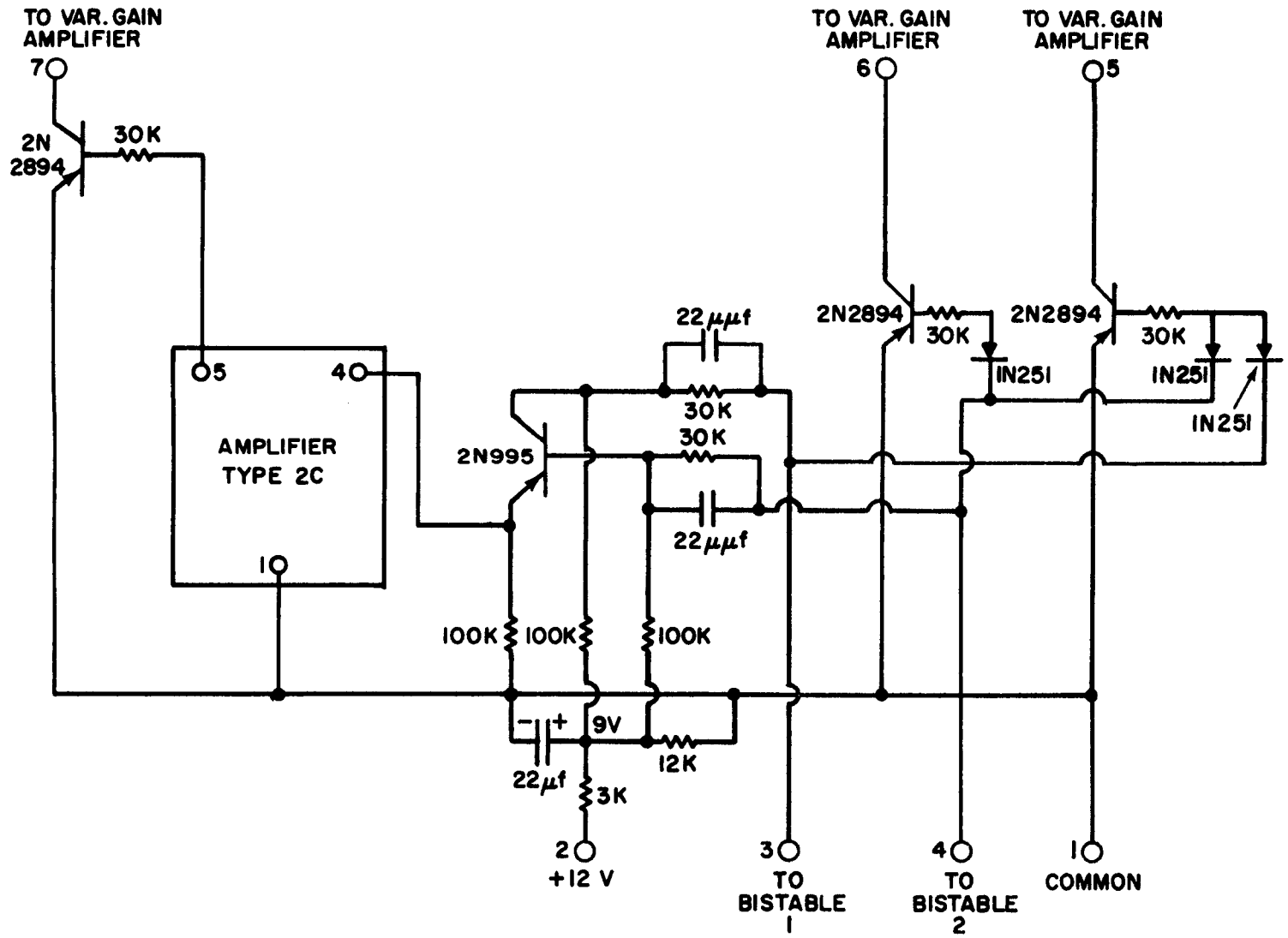


Figure 30–Attenuation Control Circuit

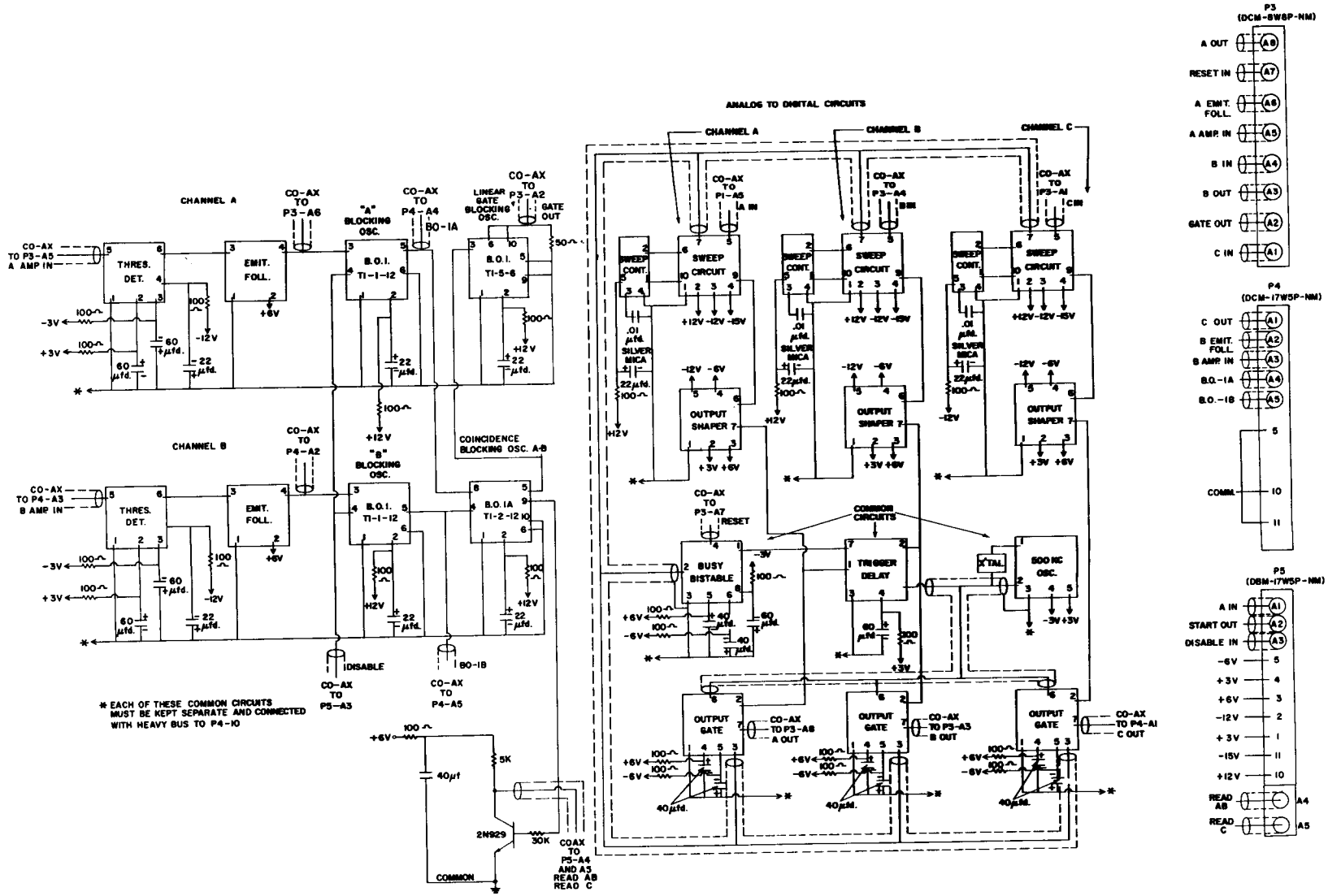


Figure 31–ADCR Mark 6 Board No. 2

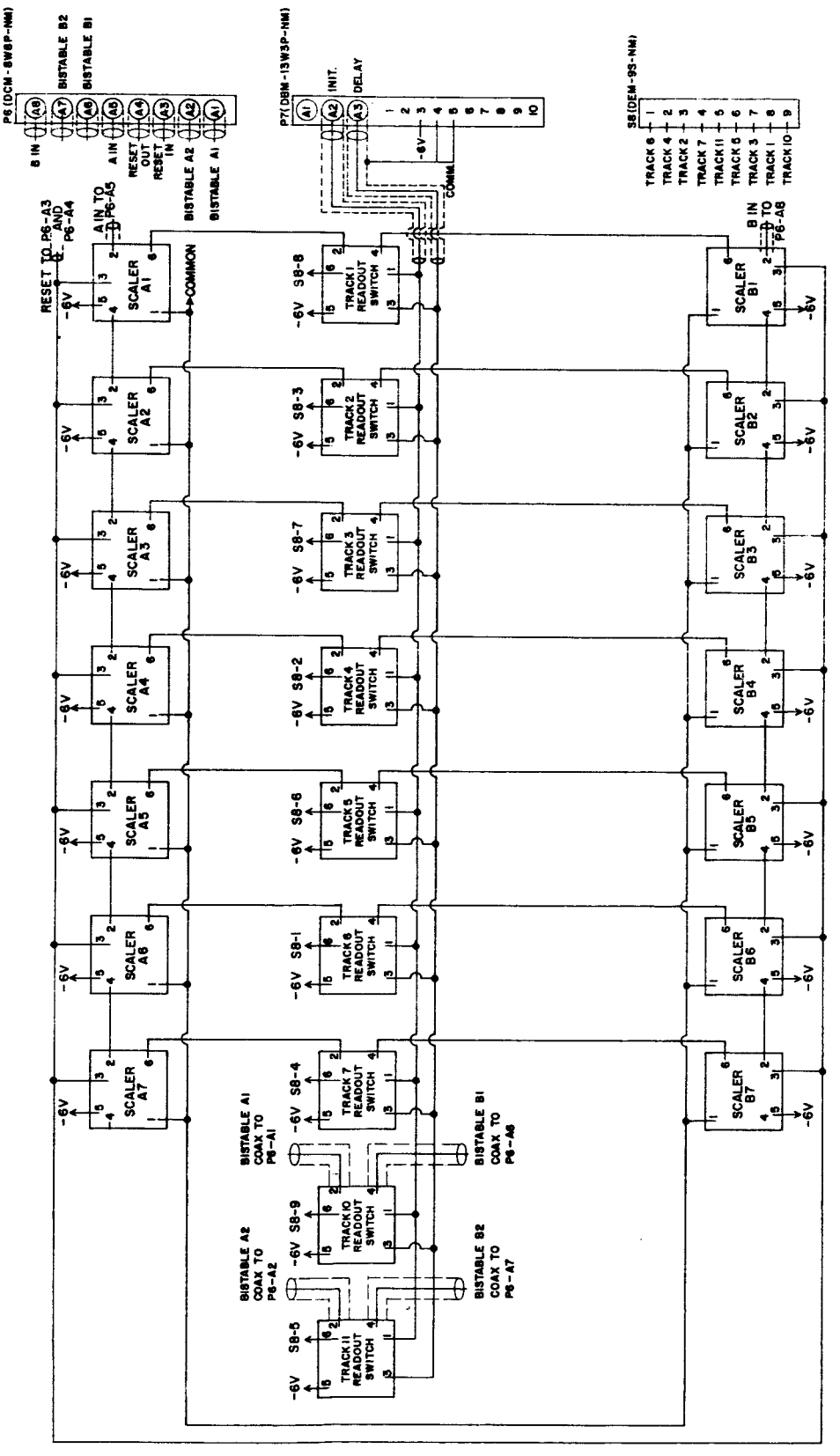


Figure 32–ADCR Mark 6 Board No. 3

Schematics of the scaler and readout switch are shown in Figure 21 and Figure 22, respectively. These circuits are connected as follows:

Initial Readout	Delayed Readout	Tape Track No.
Scaler A1	Scaler B1	1
Scaler A2	Scaler B2	2
Scaler A3	Scaler B3	3
Scaler A4	Scaler B4	4
Scaler A5	Scaler B5	5
Scaler A6	Scaler B6	6
Scaler A7	Scaler B7	7
Bistable A1	Bistable B1	10
Bistable A2	Bistable B2	11

Board No. 4. Interconnection of circuits on this board is shown in Figure 33. These circuits include:

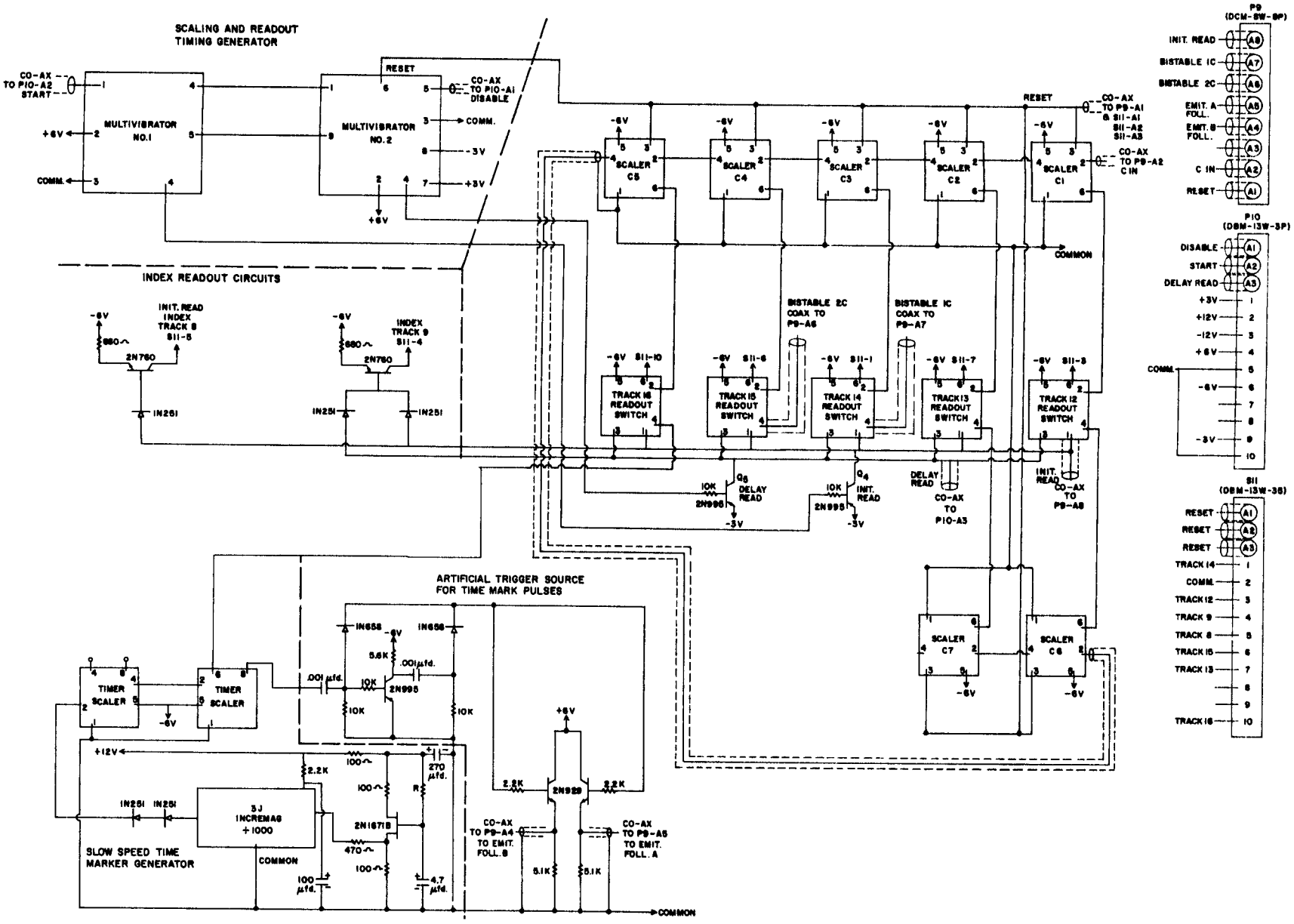
7-bit Scaler, Channel C
5 Readout Switches
Index Readout Circuits
Slow Speed Time Marker Generator
Artificial Trigger Source for Time Mark Pulses
Scaling and Readout Timing Generator

Detailed schematics of circuits on this board are in the following drawings:

Scaler, Figure 21
Readout Switch, Figure 22
Timing Generator Multivibrator No. 1, Figure 23
Multivibrator No. 2, Figure 24

1. Readout Switches, Scalers and Associated Circuits. The following table shows connection of readout switches and associated circuits:

Initial Readout	Delayed Readout	Tape Track No.
Scaler C1	Scaler C6	12
Scaler C2	Scaler C7	13
Scaler C3	Bistable 1C	14
Scaler C4	Bistable 2C	15
Scaler C5	Time Index	16
Index	No Output	8
Index	Index	9


SCALING AND READOUT TIMING GENERATOR
MULTIVIBRATOR NO.1
MULTIVIBRATOR NO.2
RESET
SCALER C5
SCALER C4
SCALER C3
SCALER C2
SCALER C1
SCALER C7
SCALER C6
COMMON
INDEX READOUT CIRCUITS
TRACK 16 READOUT SWITCH
TRACK 15 READOUT SWITCH
TRACK 14 READOUT SWITCH
TRACK 13 READOUT SWITCH
TRACK 12 READOUT SWITCH
BISTABLE 2C COAX TO P9-A6
BISTABLE 1C COAX TO P9-A7
DELAY READ
INIT. READ
ARTIFICIAL TRIGGER SOURCE FOR TIME MARK PULSES
TIMER SCALER
SLOW SPEED TIME MARKER GENERATOR
3J INCREMAG ÷1000
P9 (DCM-8W-8P)
P10 (DBM-13W-3P)
S11 (DBM-13W-3S)

2. Slow Speed Time Marker Generator. A 40 cps relaxation oscillator using a 2N1671B unijunction transistor drives a magnetic core "bucket-and-ladle" type count-down device to give an output pulse at approximately 4 minute intervals. These 4-minute pulses are fed to two additional scalers to generate one pulse every 16 minutes. This time marker pulse is recorded on tape track No. 16.

3. Artificial Trigger Source for Time Mark Pulses. A time mark pulse every 16 minutes actuates the artificial trigger source circuit and gives simultaneous output pulses on emitter followers A and B. These pulses are fed to the coincidence blocking oscillator A·B on Board No. 2, resulting in a scaling and readout action with a sensitivity bit on the delayed readout on track 16, and index bits on tracks 8 and 9. The probability of signals occurring in the pulse height analyzer channels to coincide with the time mark pulses is very low, consequently these artificially triggered readouts will nearly always be zero on the data tracks.

4. Scaling and Readout Timing Generator. The "start" signal from the coincidence blocking oscillator A · B on Board No. 2 is fed to the input of the timing generator multivibrator No. 1. This stage furnishes the "initial readout" pulse to transistor Q4 which in turn drives the readout switches and index readout circuits on Board No. 4 and the readout switches on Board No. 3. The second timing generator multivibrator fires at the end of the complete cycle from multivibrator No. 1 and furnishes the "delayed readout" pulse to transistor Q5. This transistor drives the readout switches and index readout circuits on Board No. 4 and the readout switches on Board No. 3 for the delayed readout. A rectified d-c voltage is fed to the "disable" output during the entire switching interval of both multivibrators. This voltage disables the A blocking oscillator and the B blocking oscillator on Board No. 2 during a scaling and readout action.

A reset signal at the end of each complete scaling and readout action is fed from multivibrator No. 2 to scalers on Board No. 4, scalers on Board No. 3, and the busy bistable on Board No. 2.

Board No. 5. Interconnection of circuits on this board is shown in Figure 34. These circuits include portions of the gain selecting systems for Channel A and Channel B. Schematics for these circuits are included in Figure 12.

Board No. 6. Interconnection of circuits on this board is shown in Figure 35. These circuits include a portion of the gain selecting system for Channel C, and the linear gates for channels A, B, and C. For schematics of circuits on this board, refer to Figures 5, 12, and 13.

Cable Harness and Interconnections

The cable harness and interconnections for the ADCR Mark 6 system are shown in Figure 36. Cable CA-1 interconnects the four circuit boards, the heater control circuit, the battery-power converter pack, and the tape recorder. Cable CA-2 connects the arming plug to the battery-power converter pack.

Digital Output Word Format

Each time the ADCR Mark 6 system performs an A. to D. action on pulses in channels A, B, and C, the scaling and readout action is recorded as two 16-bit words on the 16 track magnetic tape. Information carried in each bit is identified according to the format in Table 6.

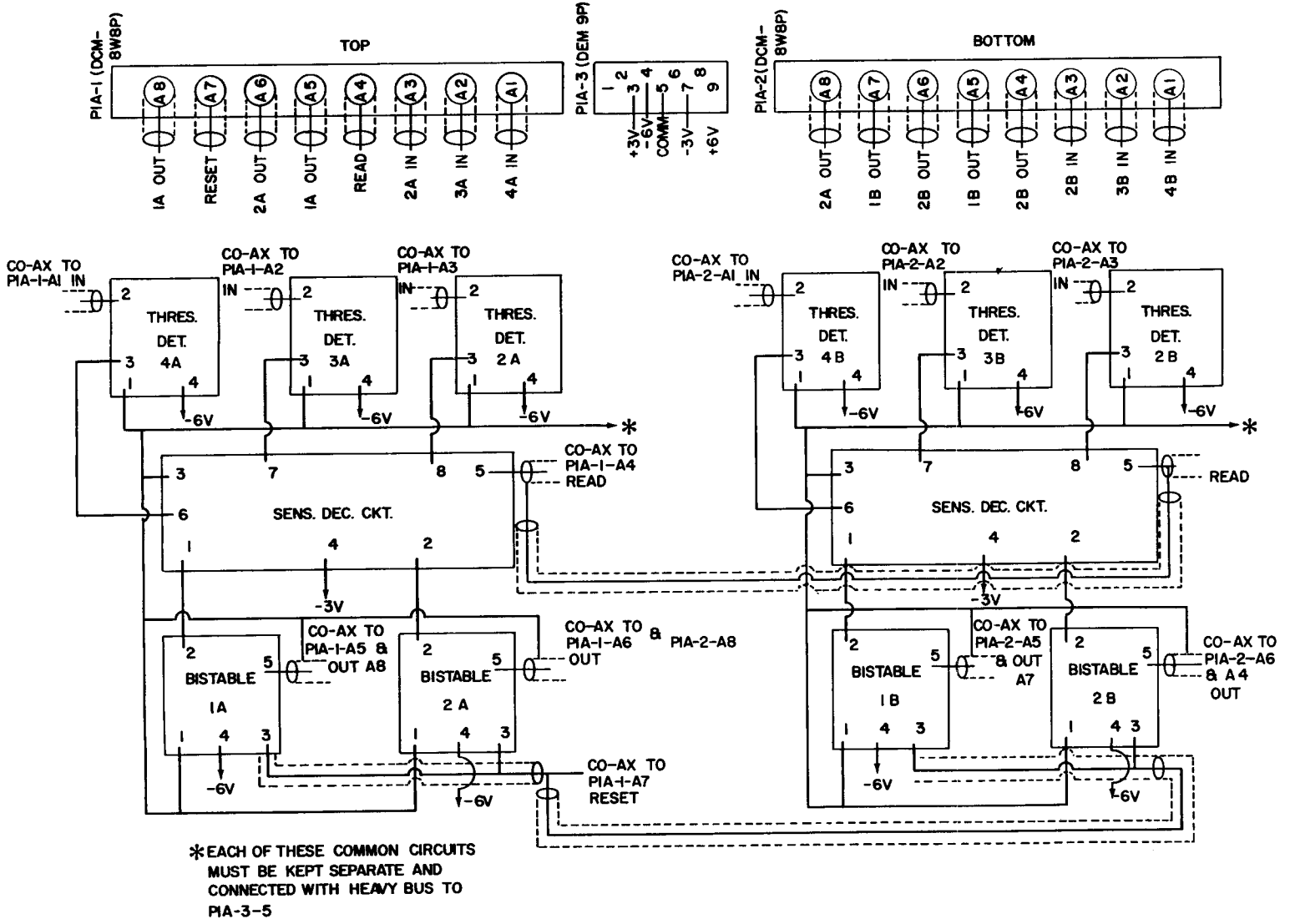


Figure 34–ADCR Mark 6 Board No. 5

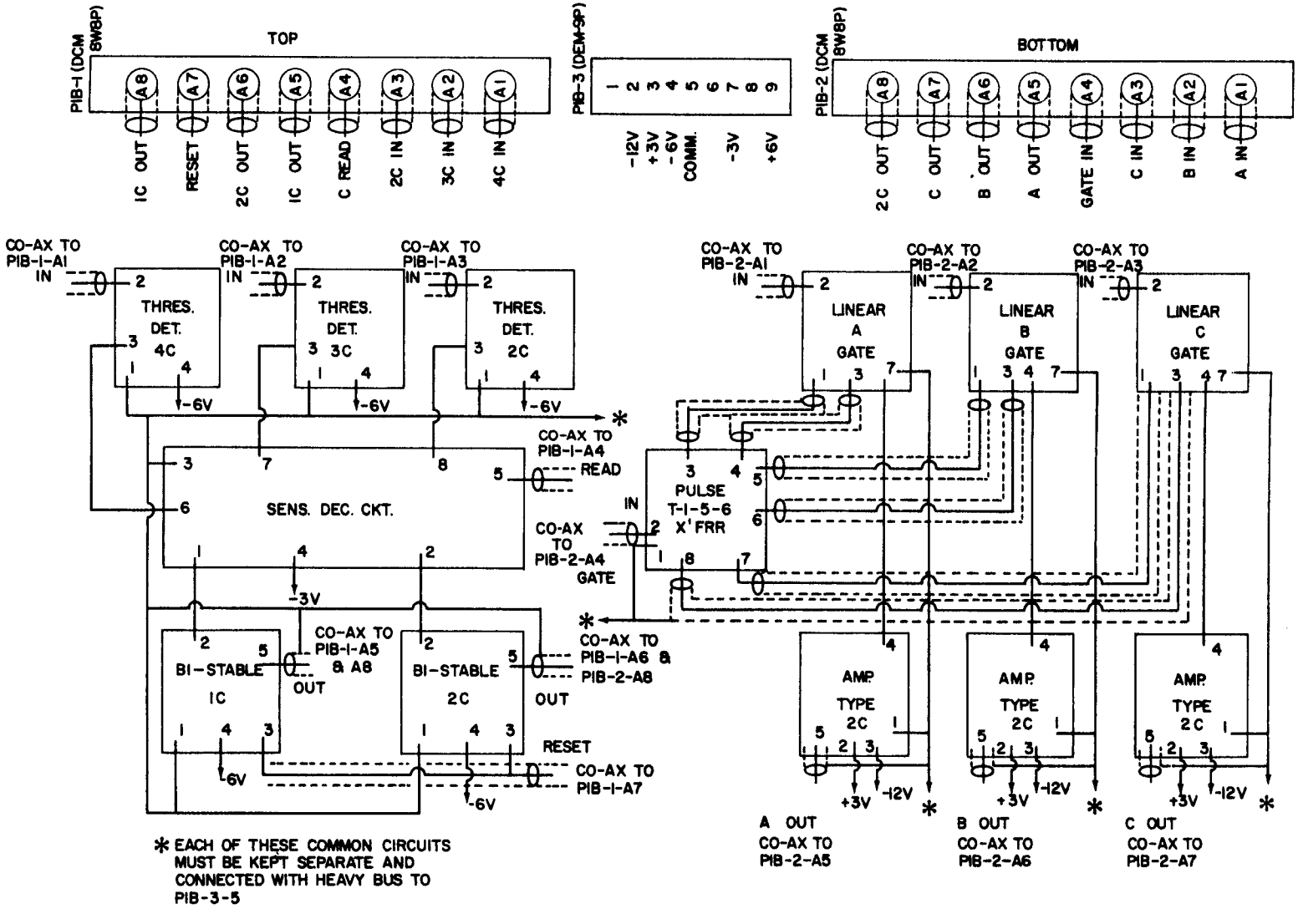


Figure 35–ADCR Mark 6 Board No. 6

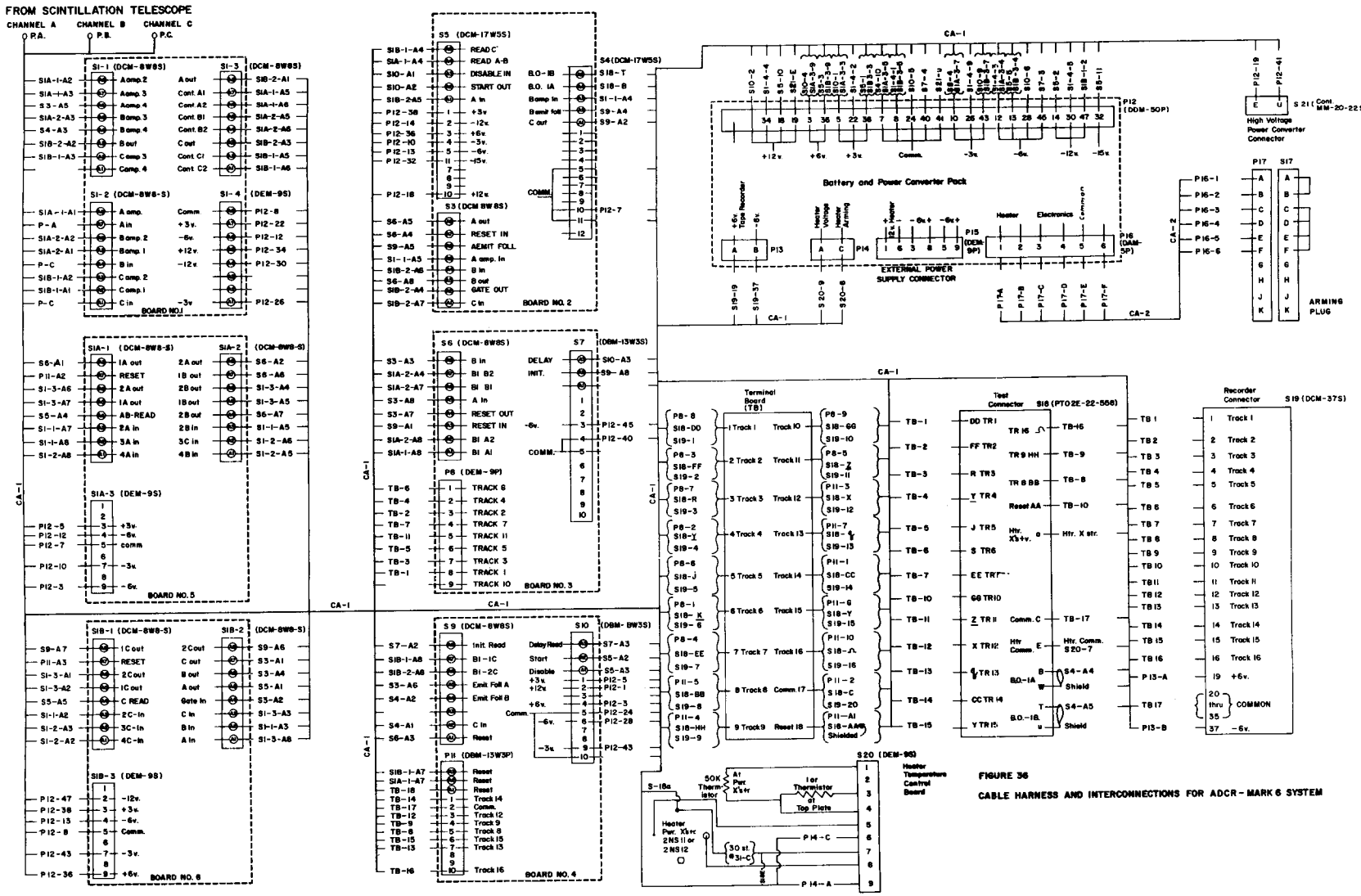


FIGURE 36

CABLE HARNESS AND INTERCONNECTIONS FOR ADCR - MARK 6 SYSTEM

Table 6
Digital Output Word Format

Track Number	Initial Readout	Delayed Readout
1	Bit A1	Bit B1
2	Bit A2	Bit B2
3	Bit A3	Bit B3
4	Bit A4	Bit B4
5	Bit A5	Bit B5
6	Bit A6	Bit B6
7	Bit A7	Bit B7
8	Index	No output
9	Index	Index
10	Multiplier A1	Multiplier B1
11	Multiplier A2	Multiplier B2
12	Bit C1	Bit C6
13	Bit C2	Bit C7
14	Bit C3	Multiplier C1
15	Bit C4	Multiplier C2
16	Bit C5	Time Index